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Application Note:

Electrical Threats and Protection of Ethernet

Board designers often use TVS Diode Arrays to provide protection for an Ethernet port. In many cases the designer uses protection to maintain equipment reliability against four main threats:

Lightning Induced Surges (IEC61000-4-5, GR-1089, ITU)

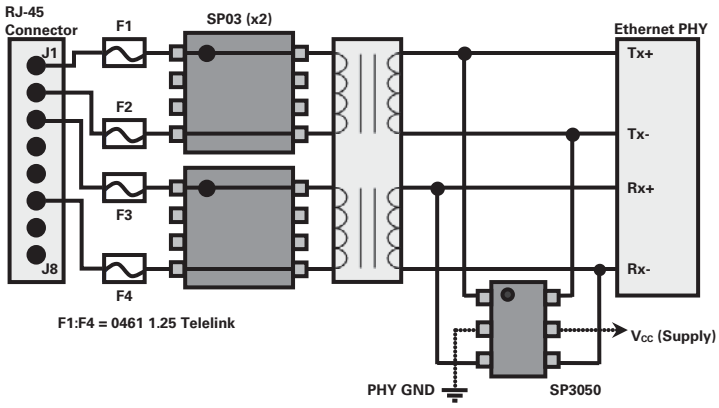
ESD or Electrostatic Discharge (IEC61000-4-2)

EFT or Electrical Fast Transient (IEC61000-4-4)

CDE or Cable Discharge Event

Understanding the nature and "directionality" of the events listed above will help guide the designer in how to best protect an Ethernet port, and more importantly, how the device's pin connections will affect system performance. The information provided in the following sections, will reference Figure 1 to help better illustrate some of the points.

Figure 1



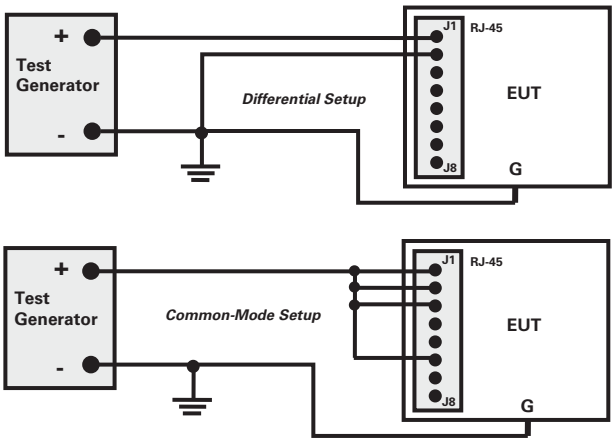
Understanding the Threat

Lightning Induced Surges

Depending on the standard or regulations being adhered to, lightning surges can be differential or common-mode with varying waveshapes. In differential mode two conductors or pins (i.e. J1 and J2) are connected between the positive and negative test equipment terminals so the energy inserted at the RJ-45 port appears only between these two conductors (see Figure 2). The energy will be dissipated in the line side protection device shown here as Littelfuse's SP03 Series, Silicon Protection Array, but some of the energy will also pass into the transformer creating a differential event on the driver side of the transformer, or between the Tx+ and Tx- data lines in this example.

For common-mode testing the individual conductors or data lines themselves will be tested with respect to GND. The positive end of the test equipment will connect to all of the conductors or pins (i.e. J1, J2, J3, and J6) and the negative terminal will be tied to GND (see Figure 2). In this case, very little energy will be dissipated in the SP03 assuming the line impedances are closed matched. The majority of the energy will be capacitively coupled through the transformer's magnetics to the driver side of transformer appearing as a common-mode event to the Ethernet PHY.

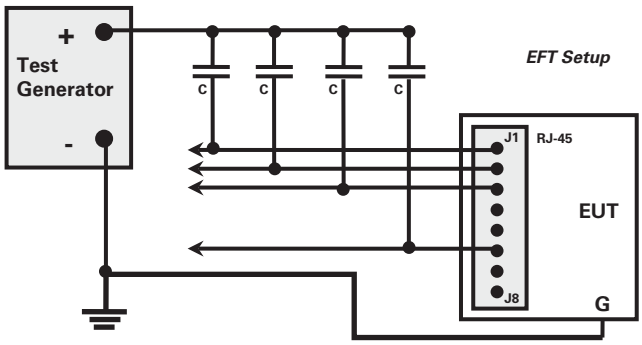
Figure 2



Electrostatic Discharge (ESD)
Equipment being evaluated for immunity to ESD (per the IEC61000-4-2 standard) can be conducted via contact or air discharge. There are numerous methods to inject ESD, but in all cases the ESD pulses appear as common-mode events to the circuit as the discharged energy is reference to GND.

Electrical Fast Transient (EFT)
Equipment being examined for immunity to EFT (per the IEC61000-4-4 standard) is very similar to the testing done for common-mode lightning surges. In the more typical configuration shown in Figure 3, all the conductors (or pins) are capacitively coupled to the positive terminal of the test generator and "surged" with respect to GND. If the data lines are well balanced there will be little to no differential energy between the pairs, but again the transformer's coupling capacitance will transfer the common-mode energy to the driver side albeit at a reduced level.

Figure 3

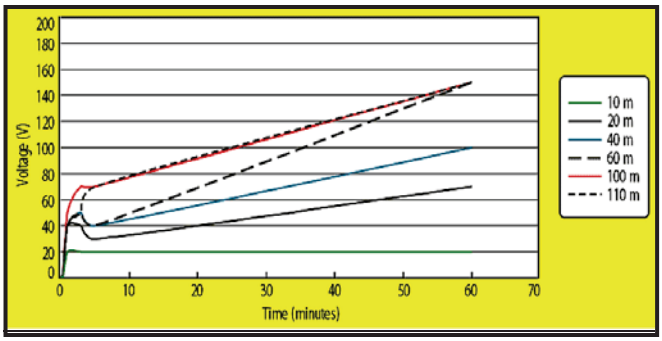


Cable Discharge Event (CDE)
CDE is a phenomenon that should be differentiated and considered separately from electrostatic discharge (ESD). The characteristics of a twisted-pair cable and knowledge of its environment play an important role in understanding CDE. The frequently changing cable environment also adds to the challenge of preventing CDE damage. A system designer can maximize protection against CDE through good layout practices and a careful selection of components. The IEEE 802.3 standard calls out isolation voltages of 2250 V_{DC} and 1500 V_{AC} to prevent connector failures that can be caused by the high voltages generated from CDEs. To prevent arcing during these events, these isolation requirements apply to the RJ-45 connector as well as to the isolation transformers. To prevent dielectric break down and sparking on the circuit board, the line side printed circuit board and the ground should have sufficient creepage and clearance between traces. Lab tests have shown that to withstand 2000V of transient voltage, the FR4 circuit board trace spacing should have a separation of at least 250 mils. (Source: www.national.com). The UTP cable discharge event can be as high as a few thousand volts and can be very destructive. The charge accumulation comes from two main sources: triboelectric (friction) effect and electromagnetic induction effect.

These effects can come from pulling a PVC-covered CAT5 UTP cable on a nylon carpet that can cause charge build up on the cable. In a similar way, charge can also build up on a cable when the cable is pulled through a conduit or dragged through other network cables. This charge build up is similar to that from scuffing of feet across a carpet. The charge build up only occurs when the cable is un-terminated and the charge is not immediately dissipated (i.e. both ends of the cable are not plugged into a system). Also, the accumulated charge has to be retained in order to cause substantial damage. The newer CAT5 and CAT6 cables have very low dielectric leakage and tend to retain charge for a long period. Charge retention time is increased in an environment where there is low relative humidity. When a charged UTP cable is plugged into a RJ-45 network port, there are many possible discharge paths. This transient current takes the lowest inductance path and this path could be at the RJ-45 connector, between two traces of a printed circuit board (PCB), in the transformer, through the Bob Smith AC termination, or through the silicon device. Depending on the length of the cable, the accumulated charge can be hundred times larger than a typical ESD model charge.

This ensuing high-energy discharge may damage the connector, the transformer circuit, or the Ethernet transceiver. The twisted-pair cable behaves like a capacitor by storing a charge. Studies have proven that several hundred volts of charge can accumulate on an unterminated twisted-pair cable. Plus, a fully discharged cable can build up half of its potential charge within one hour. Once charged, a high-grade cable can retain most of its charge for more than 24 hours. How different lengths of a CAT5 cable can charge up over time is illustrated in Figure 4 below. Because longer cables have the capacity to store more charge, extra CDE precautions should be taken with systems that have cable lengths greater than 60m.

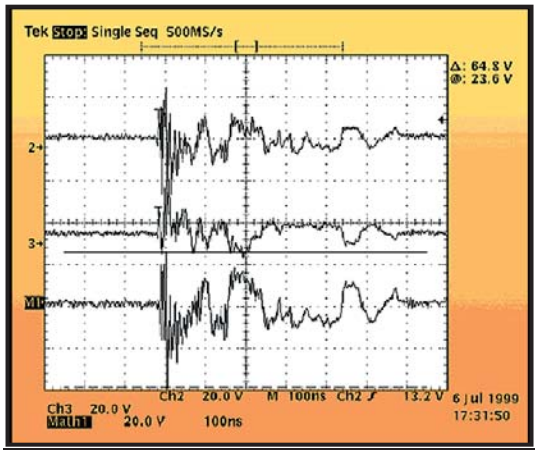
Figure 4



Another important factor to understand is the CDE waveform since it's unlike any threat previously discussed in that in can be either differential or common-mode depending on the coupling mechanism. Furthermore, preliminary studies reveal that it can have wide variations in characteristics, yet in general terms, the CDE waveform has high energy and exhibits both voltage and current drive. The waveform is spread out in time over hundreds of nanoseconds with rapid polarity reversals.

Figure 5 below shows an example of a destructive CDE waveform at the transmitter pins of an Ethernet PHY, after a 25ft twisted-pair cable was charged to 1.5kV. Over 600ns of time elapse during the event while there were transitions of 64.8V from positive to negative voltage seen on the differential waveform. In this experiment, the PHY's transmitter was destroyed and unable to transmit packets on the network.

Figure 5



From the perspective of the board-level designer, Ethernet systems should be designed and laid out with attention paid to CDE with primary focus placed on diverting energy away from IC devices. System design considerations include the addition of TVS Diode Arrays and the coupling transformer itself. The transformer circuit will help protect against common-mode transients, but high-energy transients should have a path to ground.

Optimal Device Configuration

Any line side protection device (SP03 in this example) cannot have its GND pins (2, 3, 6, and 7) tied to GND to comply with the IEEE802.3 standard for isolation; therefore, the designer has no choice but to leave this device as "differential only" protector. *(Note: Naturally, this necessitates the need for a driver side protection element to protect against common-mode events.)*

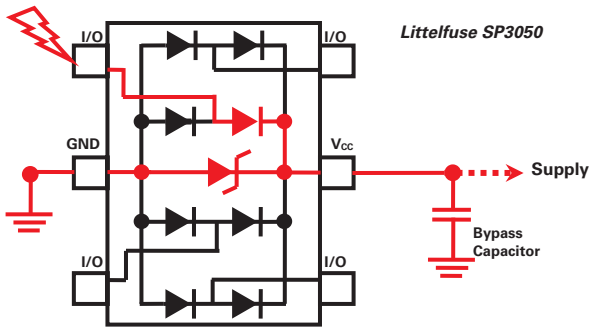
The device protecting the PHY or driver side will always have its I/O pins tied to the differential pairs as shown in Figure 1. However unlike the line side protector, this device can have its GND pin connected to the local GND plane and Littelfuse recommends this configuration. If the GND pin were not connected, then the protection device (SP3050 in this example) would become a differential only protector and would potentially allow damaging common-mode events to pass through to the PHY unclamped. Also, it should be noted that the device will still protect against differential events, even if the GND pin is connected, once the voltage difference exceeds the breakdown of the internal TVS plus two diode drops (using the SP3050 example).

As for the remaining pin commonly found on most TVS Diode Arrays, pin 5, V_{CC}, Littelfuse also recommends that this be tied to the local power supply such as 5V, 3.3V, etc. *(NOTE: Care should be taken to make sure the protection device's standoff voltage or V_{RWM} is well above the supply voltage to prevent activating or turning on the internal TVS diode.)*

By connecting the V_{CC} pin of the SP3050 the designer will get better overall clamping due to the two separate discharge paths the electrical transient would take as shown in red below (Figure 6). It can simply be thought of as a resistive divider where the transient enters through the steering diode and takes two paths, one to GND via the internal TVS and one to GND through the power supply or an external bypass capacitor. Conclusively, connecting pin 5 to the power

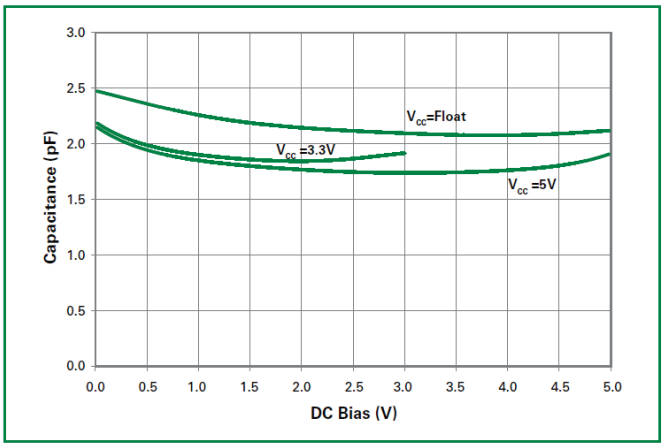
supply will result in better clamping performance providing overall better protection for the Ethernet PHY.

Figure 6



Another benefit of biasing the V_{CC} pin is that it will lower the capacitance from I/O to GND as opposed to leaving it floating or not connected. The datasheet for the particular device being used to protect the Ethernet PHY should be consulted to give the designer the value of this capacitance which will be partly dependent on the V_{CC} bias level. For reference, the plot for the SP3050 can be seen below in Figure 7.

Figure 7



Conclusion

When using TVS Diode Arrays to protect an Ethernet port, the designer should always be wary of the threats he or she is protecting against. In most all cases, the threats are a combination of differential and common-mode events that can be effectively clamped when the protection device is connected properly.

The line side protection elements are limited to differential only protection, but the driver or PHY side protection device should be connected to GND and the local power supply. This will provide the best clamping performance and maximize the reliability of the Ethernet port.

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