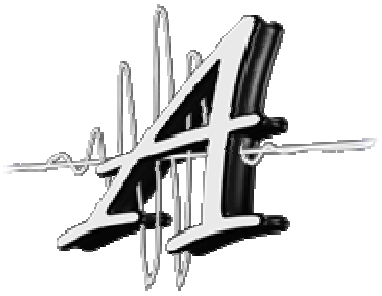
Predicting and Controlling Common Mode Noise from High Speed Differential Signals

Bruce Archambeault, Ph.D.

IEEE Fellow, iNARTE Certified Master EMC Design Engineer, Missouri University of Science & Technology
Adjunct Professor



bruce@brucearch.com

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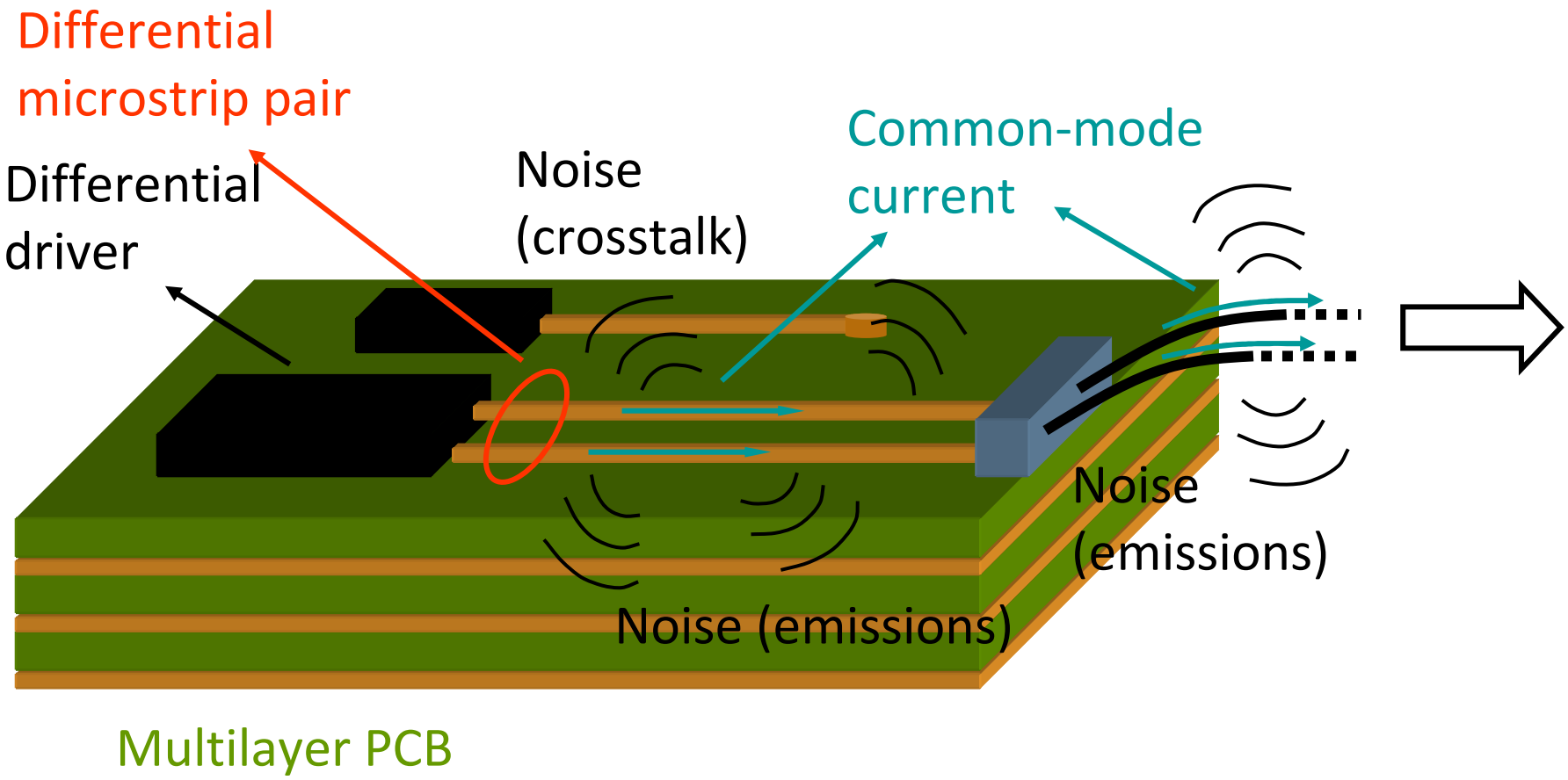
Why Control Common Mode Noise in Differential Pairs?

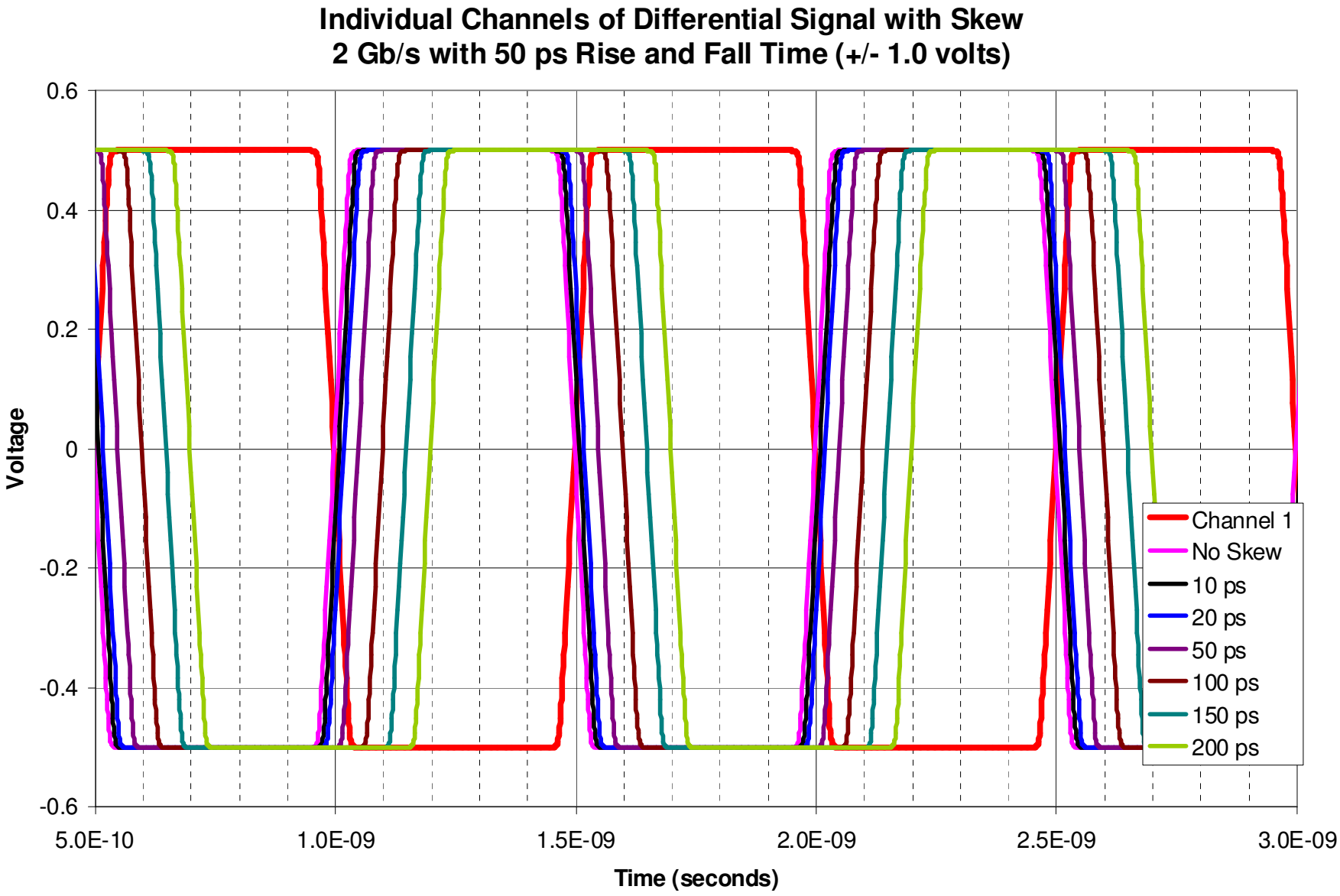
- Common Mode Noise is inevitable in differential pairs
  - Skew
  - Rise/fall time mismatch
  - Asymmetry in channel
- Common mode noise is a big problem in EMC!
- Common mode noise can increase differential crosstalk

Common-Mode Noise on PCB

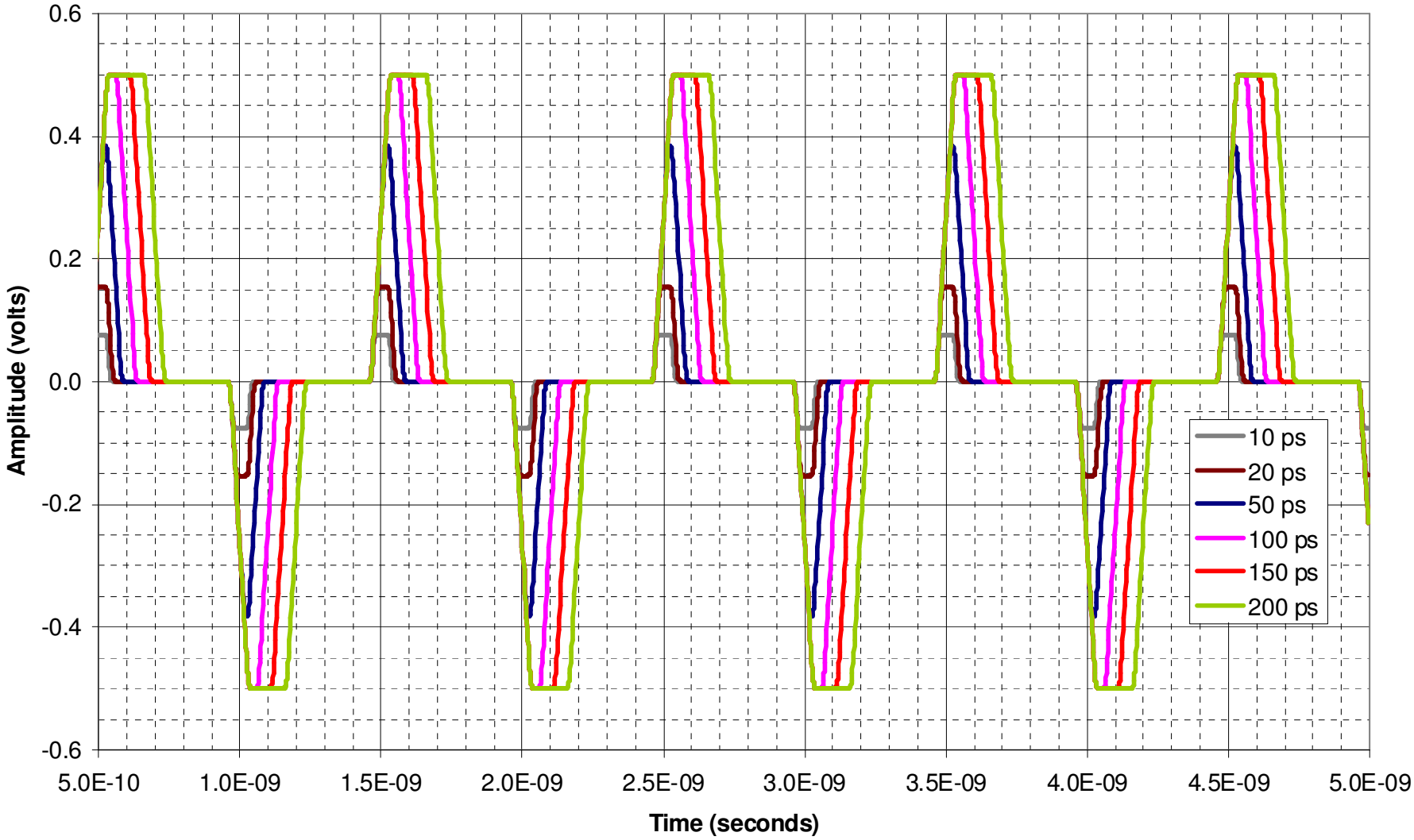


Common Mode Noise Due to Skew

- Small amounts of skew create significant common mode nose
- As little as 1% of bit width for skew can have significant EMI effects
- As little as 10% of bit width skew creates CM signal of equivalent amplitude as initial signals


Individual Channels of Differential Signal with Skew
2 Gb/s with 50 ps Rise and Fall Time (+/- 1.0 volts)
Voltage
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
5.0E-10
1.0E-09
1.5E-09
2.0E-09
2.5E-09
3.0E-09
Time (seconds)
Channel 1
No Skew
10 ps
20 ps
50 ps
100 ps
150 ps
200 ps

Common Mode Voltage on Differential Pair Due to In-Pair Skew
2 Gb/s with 50 ps Rise and Fall Time (+/- 1.0 volts)



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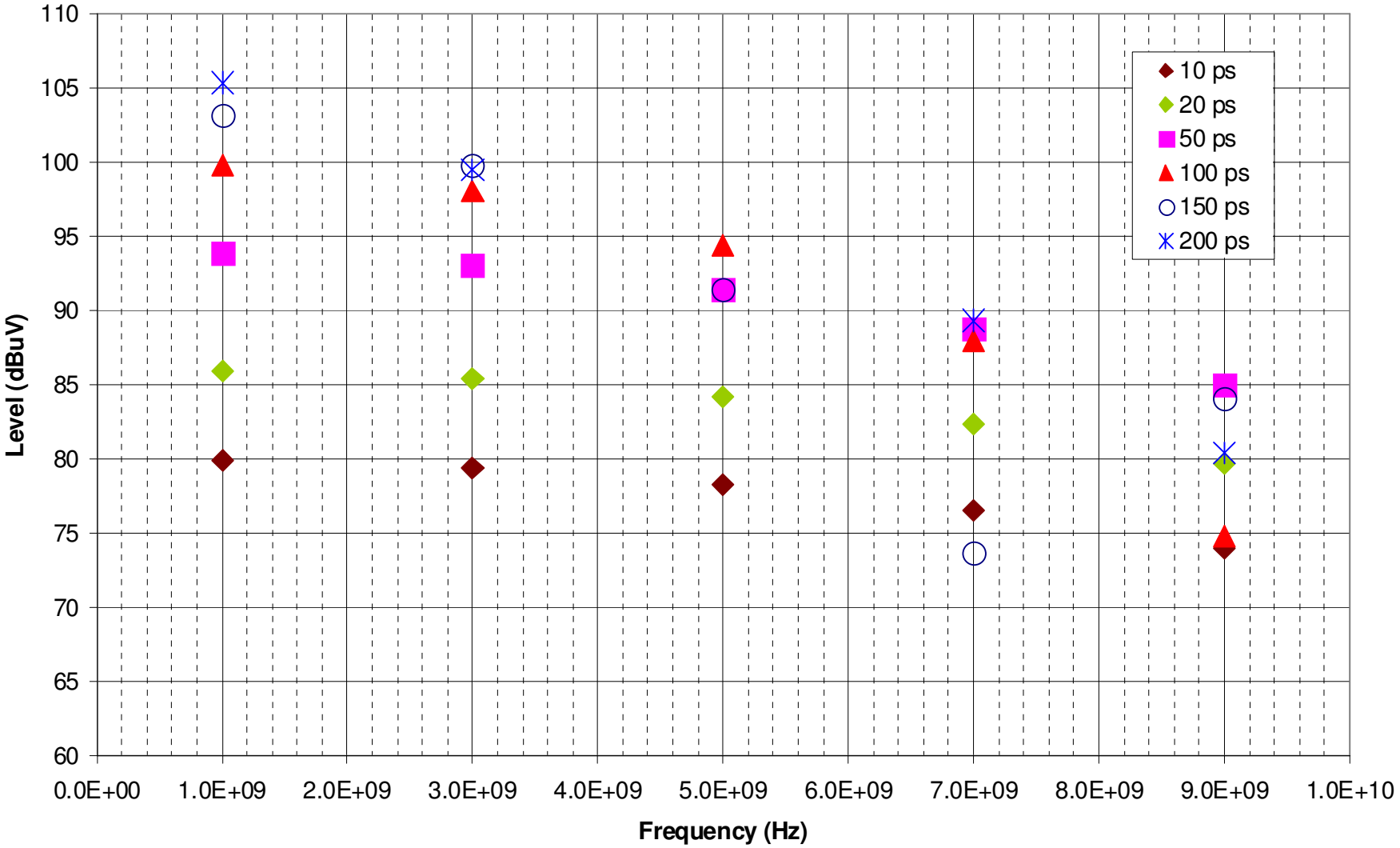
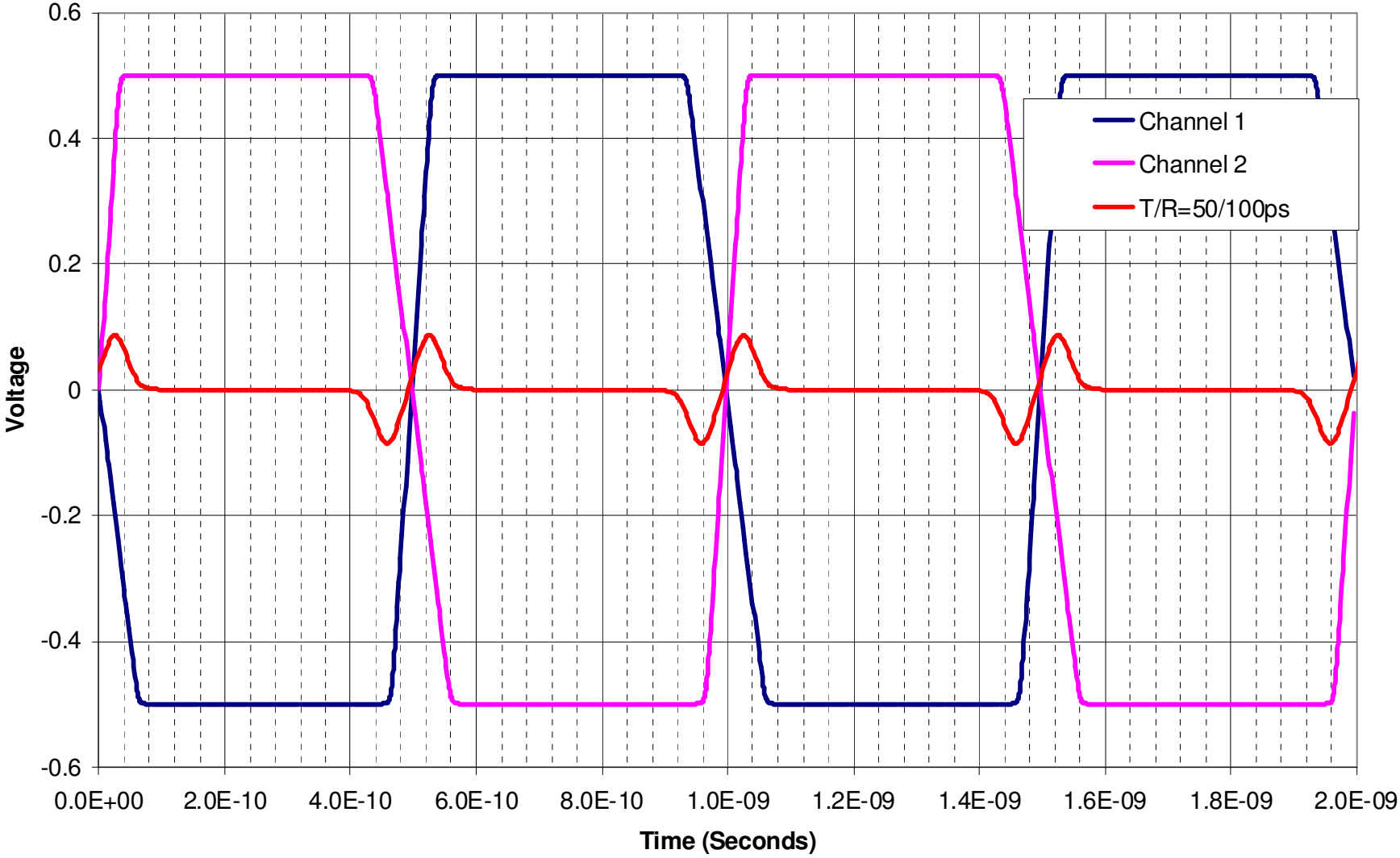


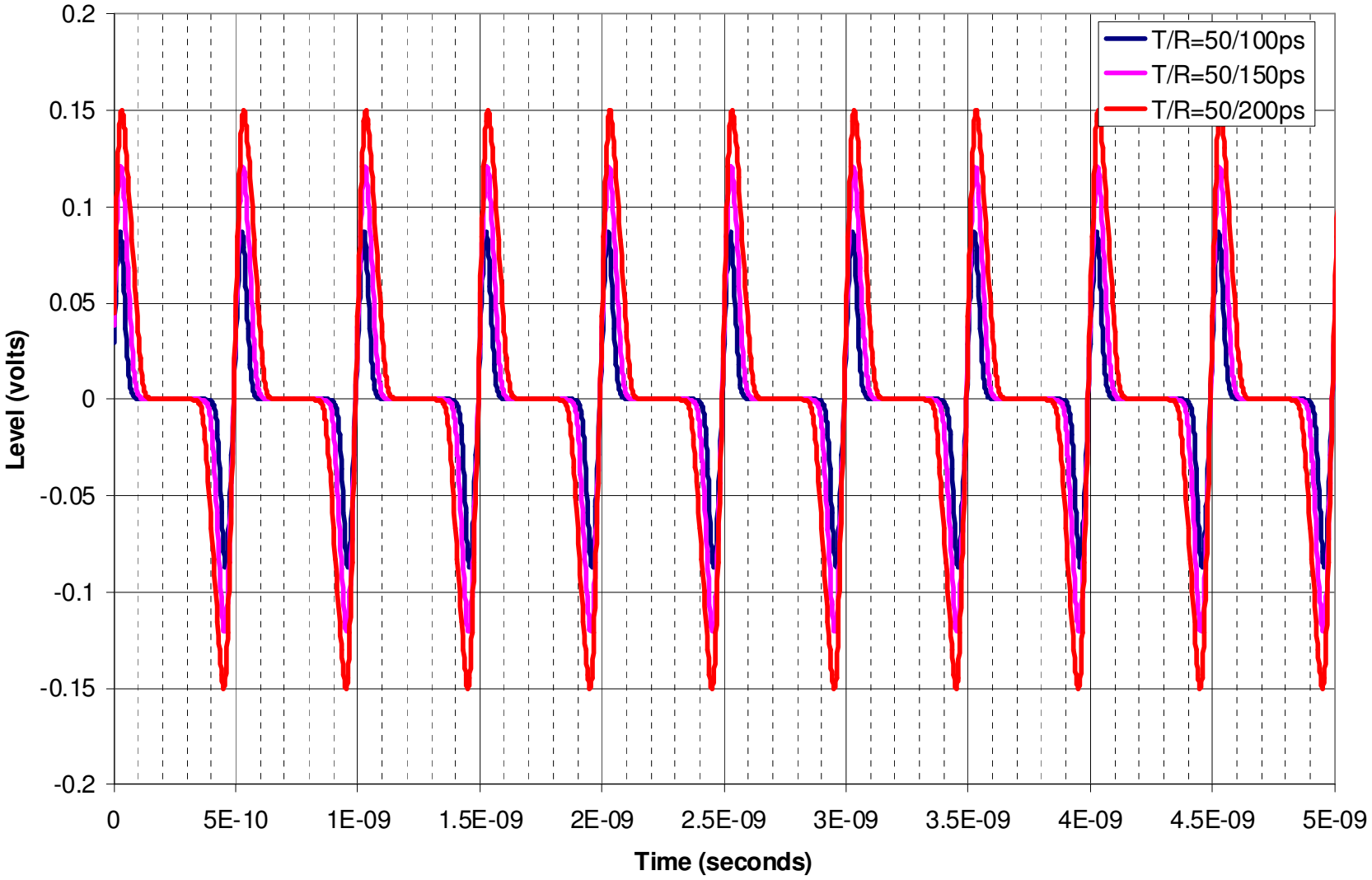
Common Mode from Rise/Fall Time Mismatch

- Small amounts of mismatch create significant CM noise
- Not as significant as skew, but harder to control!

Example of Effect for Differential Signal with Rise/Fall Time Mismatch
2 Gb/s Square Wave (Rise/Fall = 50 & 100 ps)



Common Mode Voltage on Differential Pair Due to Rise/Fall Time Mismatch
2 Gb/s with Differential Signal +/- 1.0 Volts



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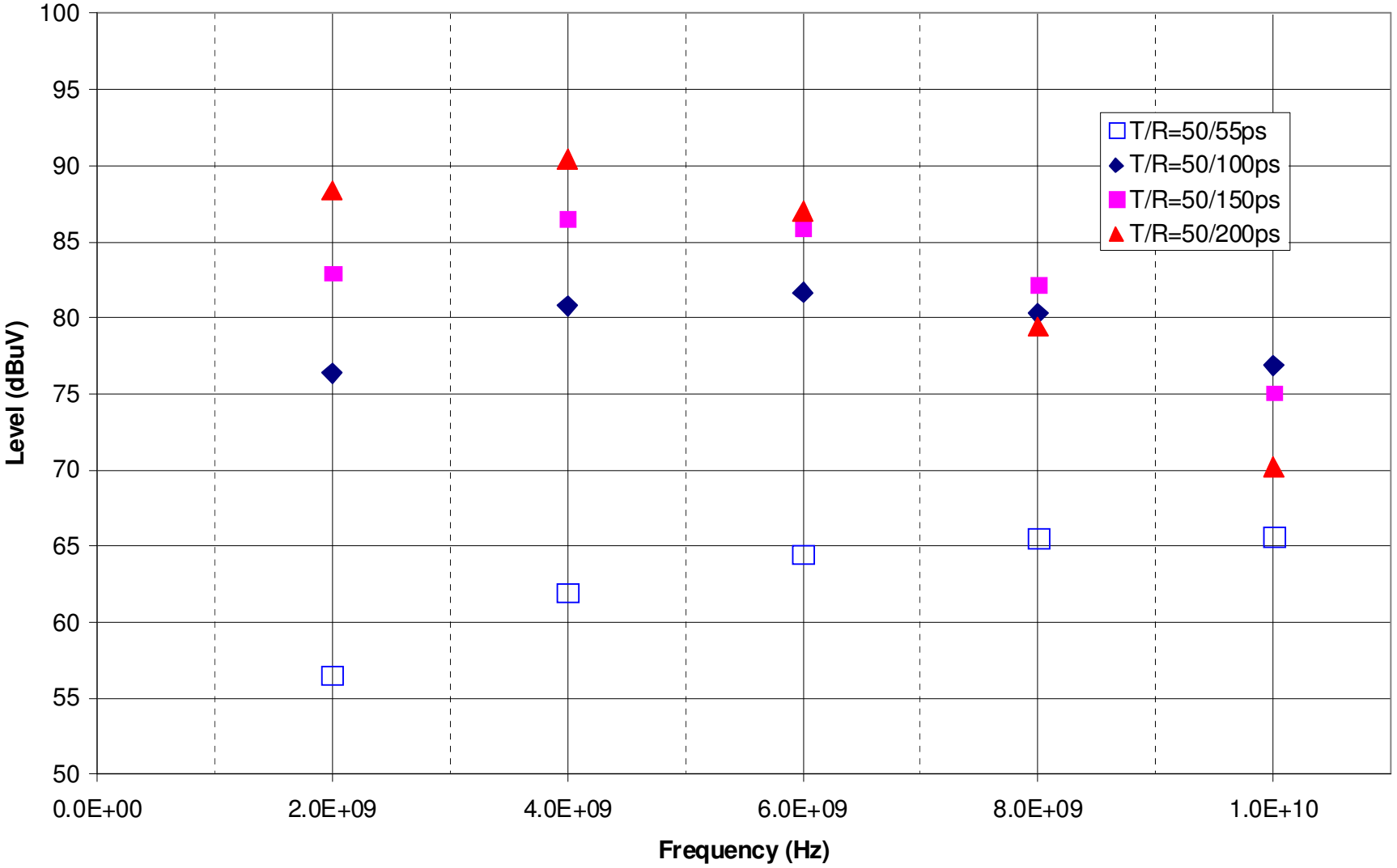
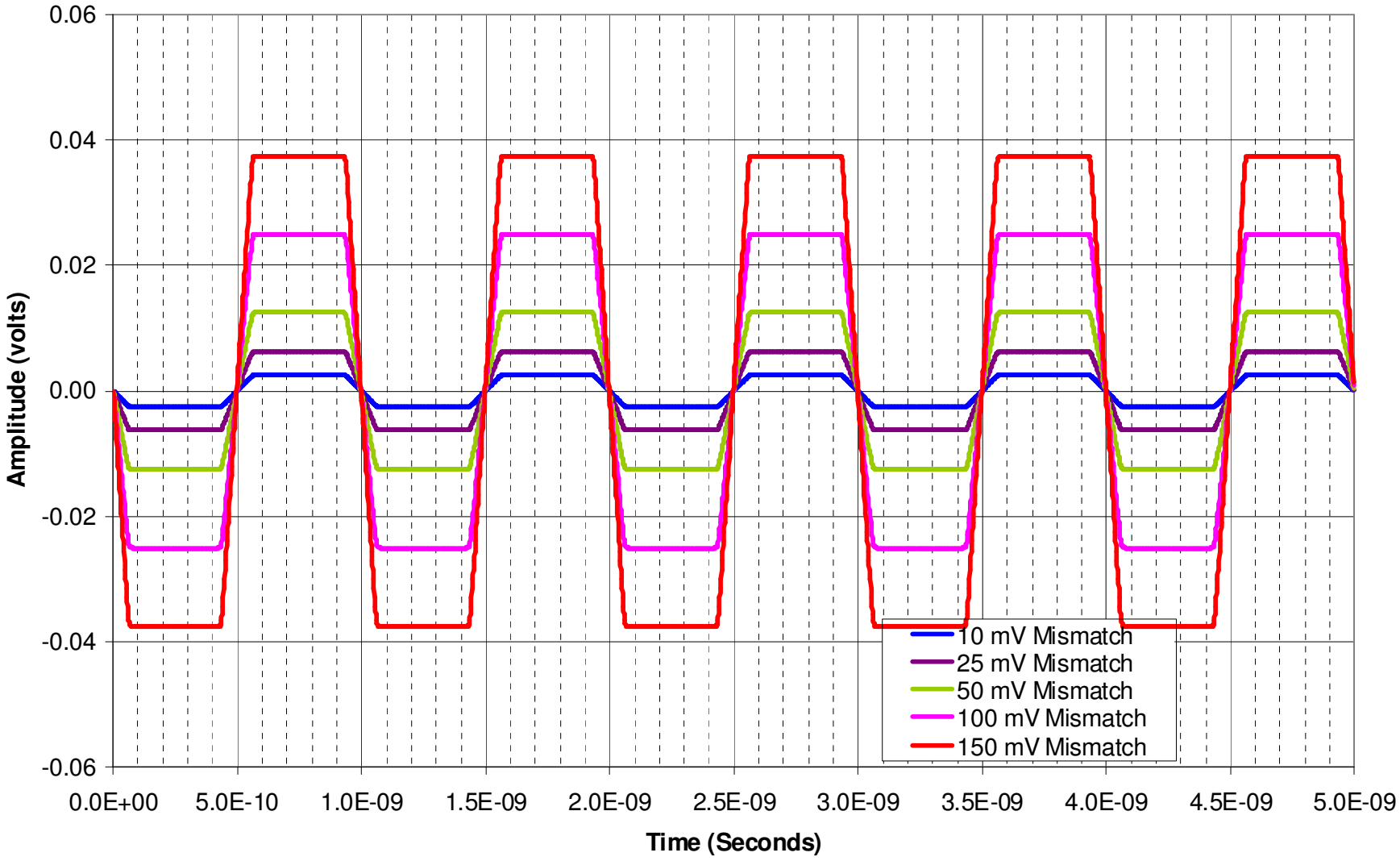


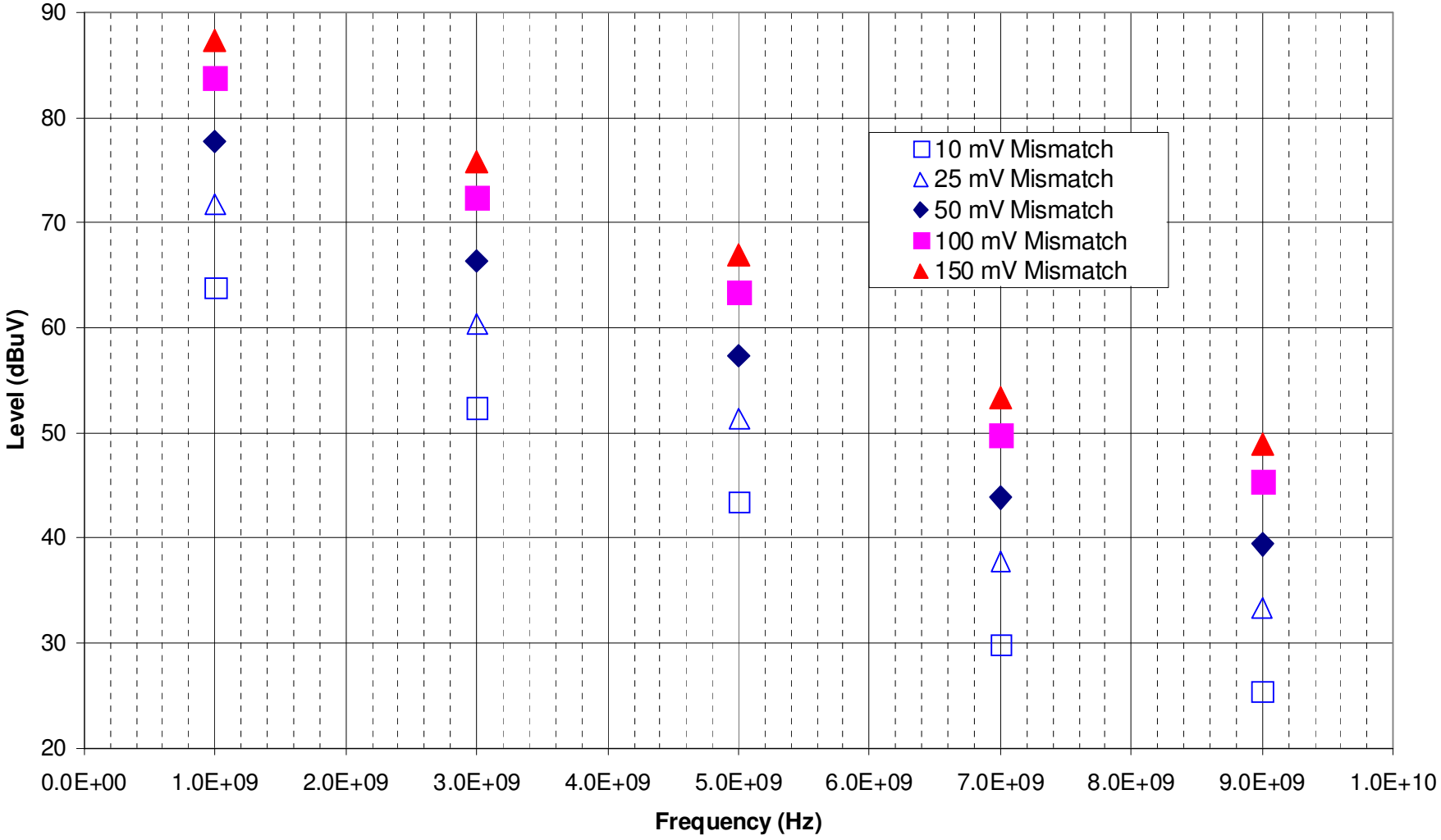
Common Mode from Amplitude Mismatch

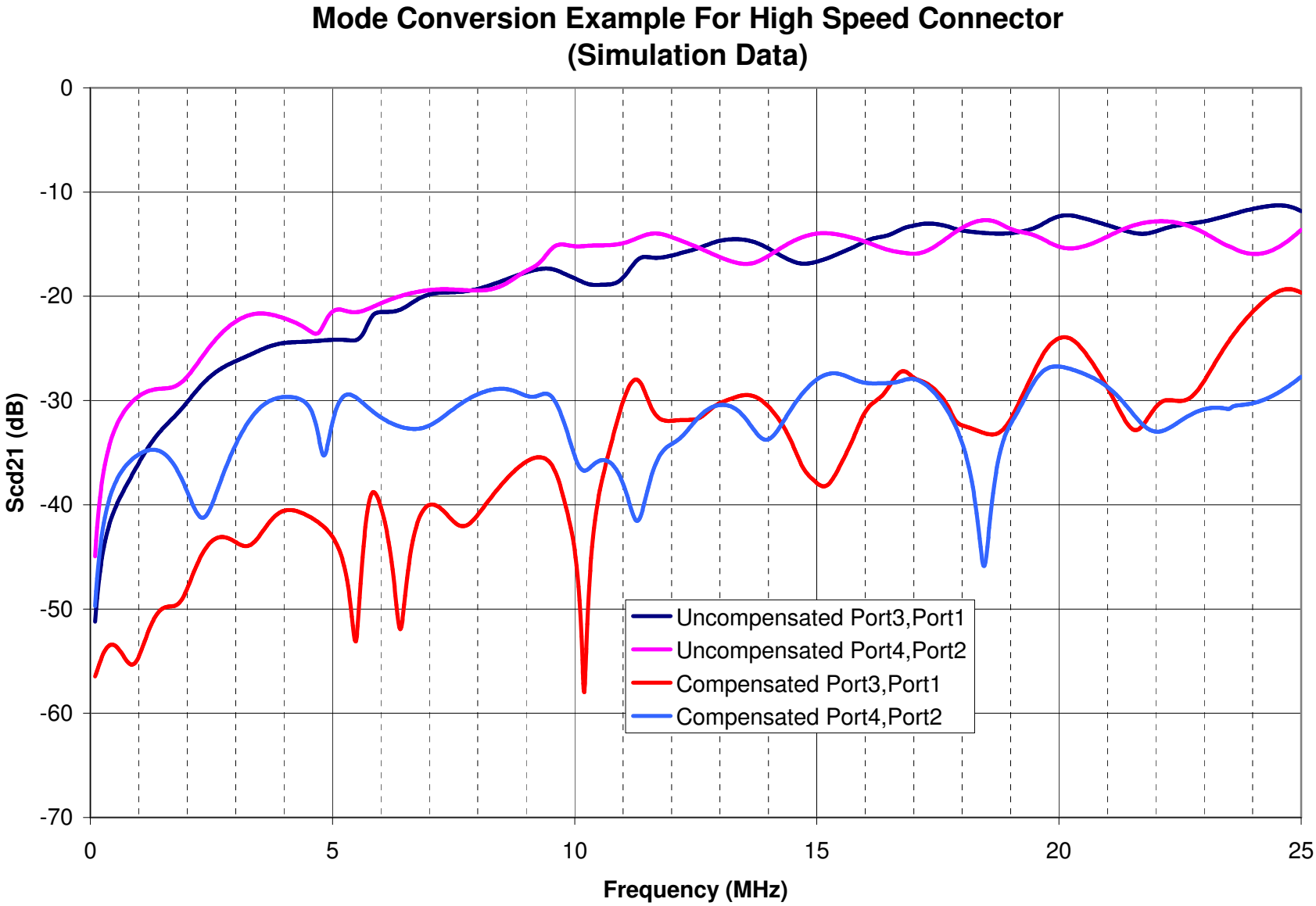
- Small amounts of mismatch create significant CM noise
- Harmonics are additive with other sources of CM noise

Common Mode Voltage on Differential Pair Due to Amplitude Mismatch
Clock 2 Gb/s with (100 ps Rise/Fall Time) Nominal Differential Signal +/- 1.0 V



Common Mode Voltage on Differential Pair Due to Amplitude Mismatch
Clock 2 Gb/s with (100 ps Rise/Fall Time)
Nominal Differential Signal +/- 1.0 Volts

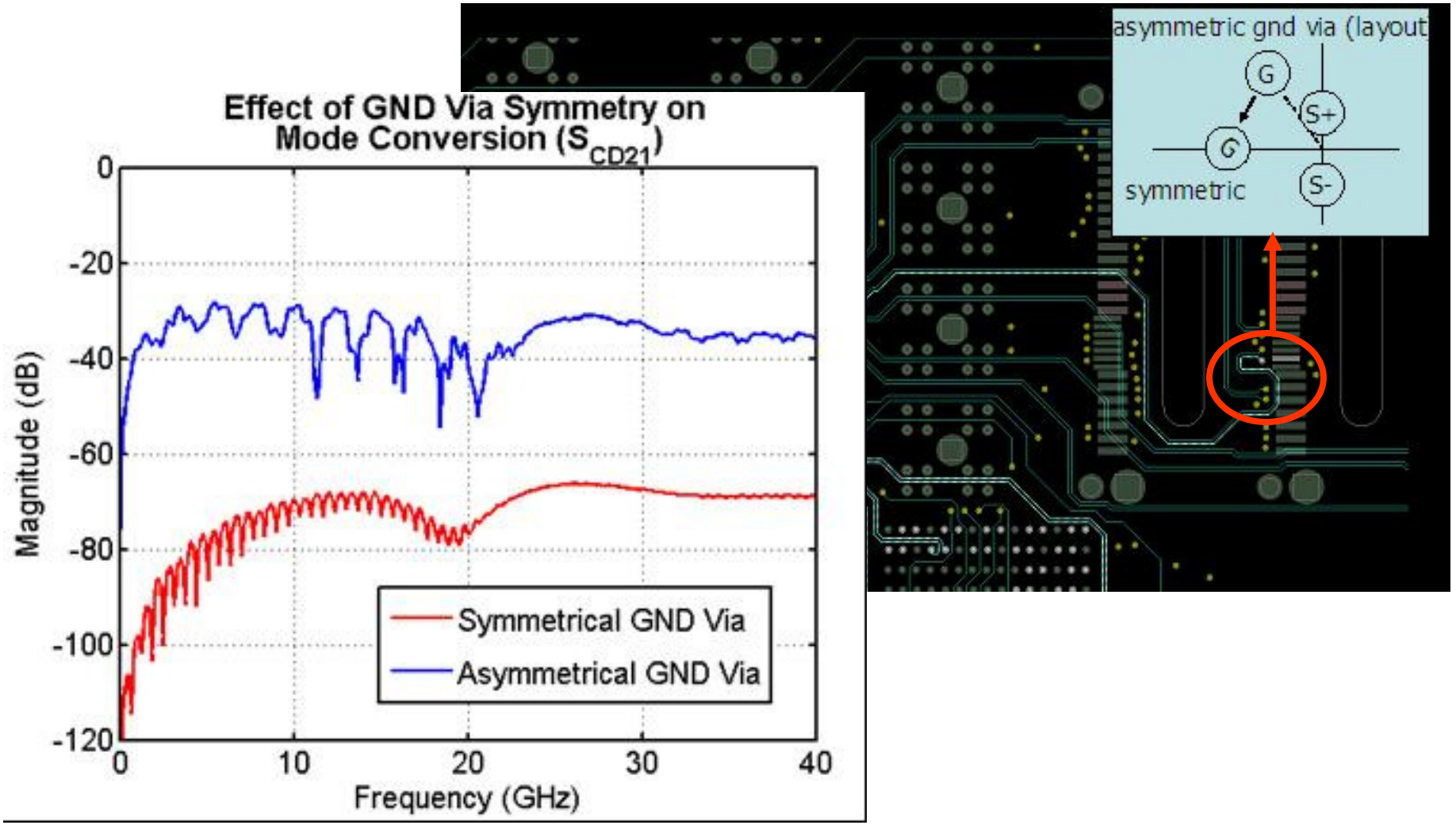



Mode Conversion Example For High Speed Connector
(Simulation Data)
Scd21 (dB)
0
-10
-20
-30
-40
-50
-60
-70
0
5
10
15
20
25
Frequency (MHz)
Uncompensated Port3,Port1
Uncompensated Port4,Port2
Compensated Port3,Port1
Compensated Port4,Port2

Compensation

- Added extra trace length before connector to compensate for connector pin mismatch
- End-to-end SI sees the improvement
- EMC does ***not*** see the improvement

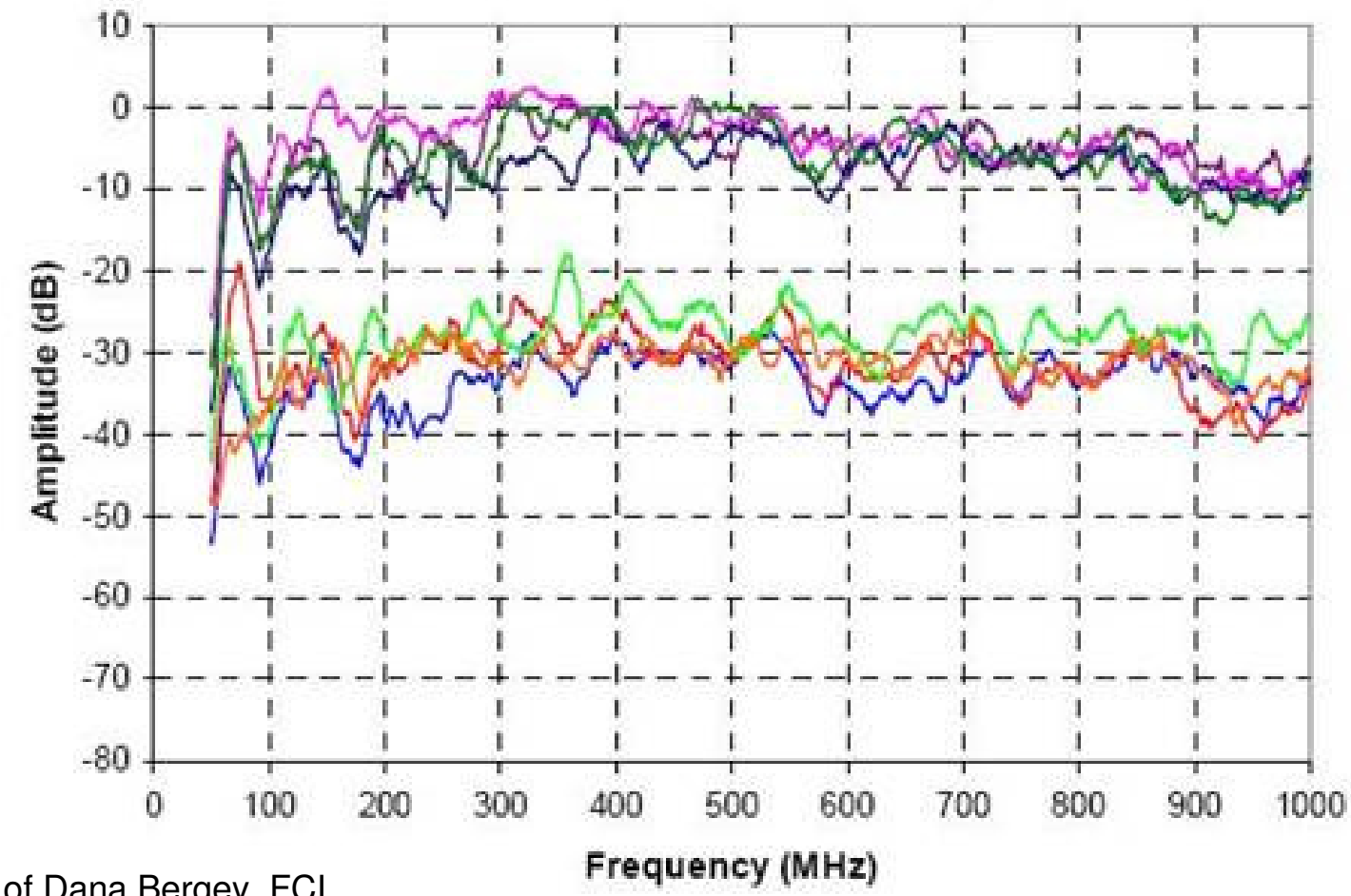
Via Symmetry Effect on Common Mode Conversion



Cable Shielding Important

- Different cables have different amounts of shielding
- Likely to vary with frequency
- May vary from vendor to vendor

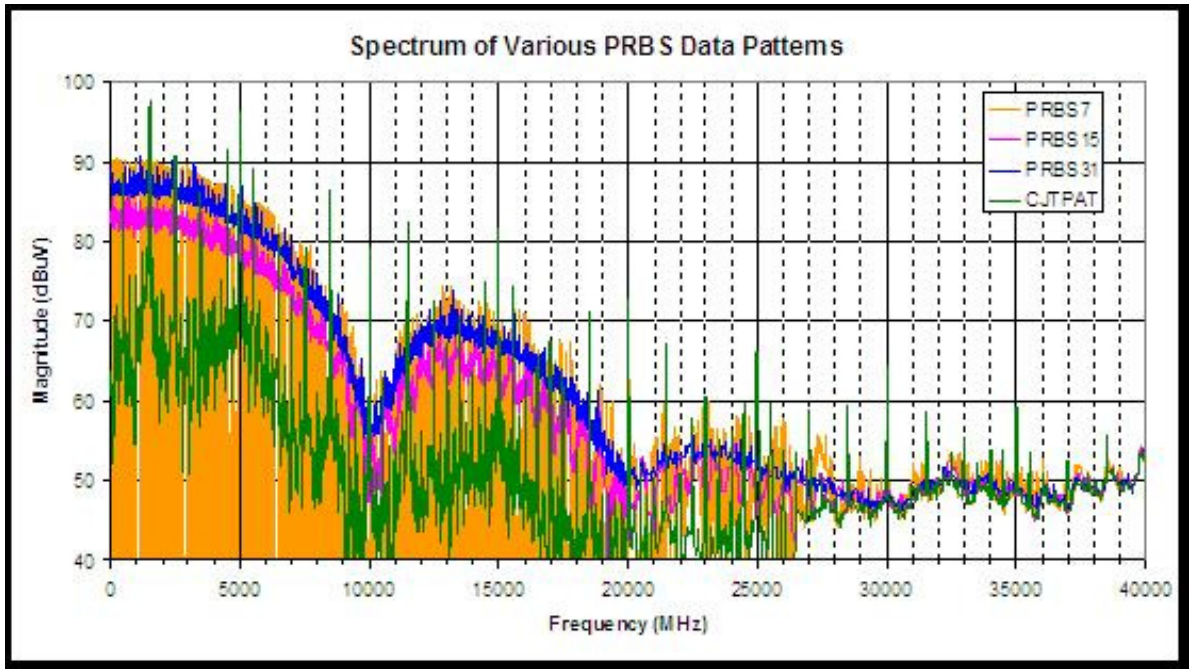
Measured Shielding Effectiveness for Various USB Cables



Courtesy of Dana Bergey, FCI

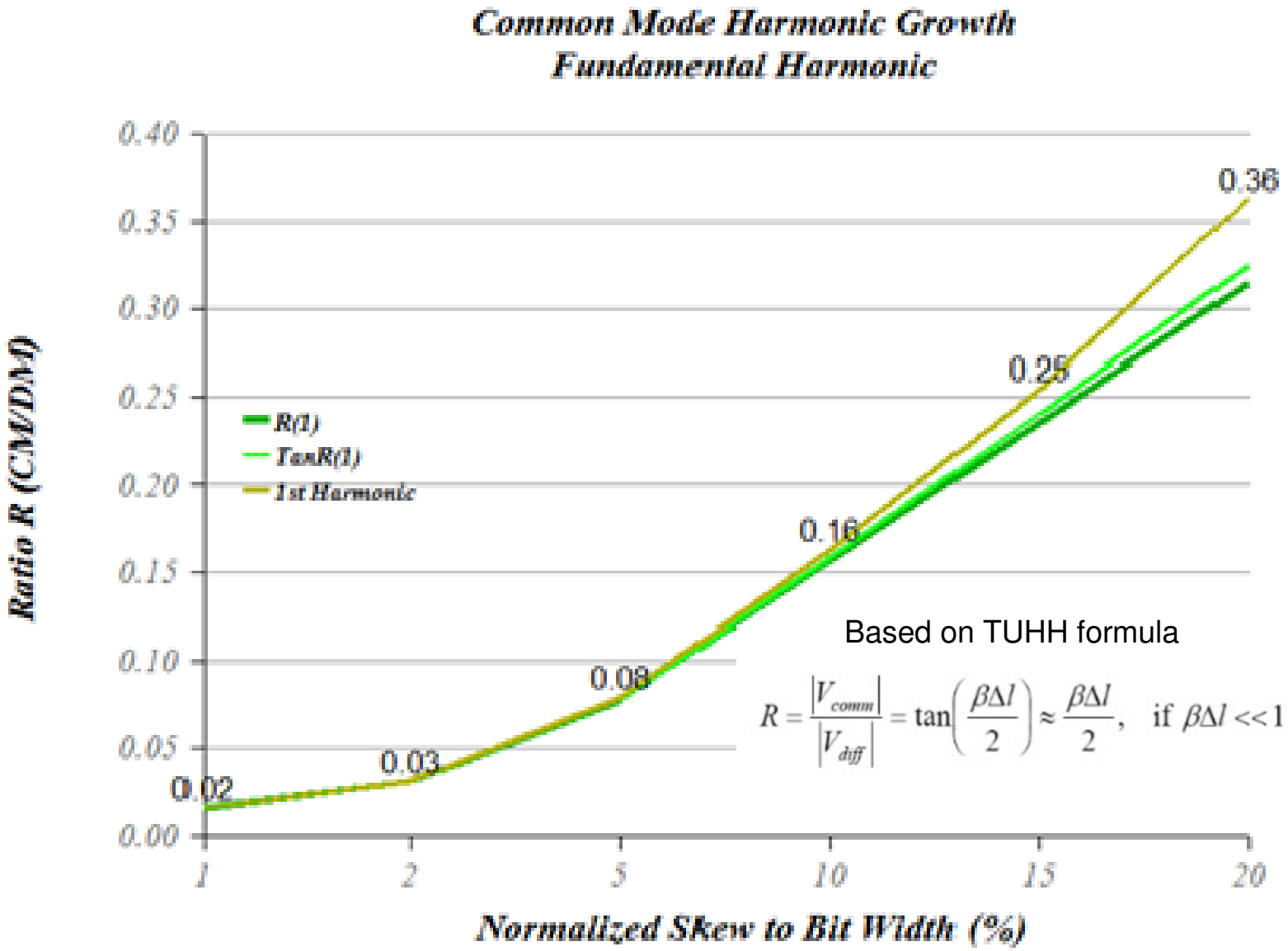
How Much is Too Much?

- Start with source amplitude
  - Near end will have full amplitude
  - 5 Gb/s



How Much is Too Much Skew?

- Most of skew comes from PCB differential trace pair mismatch
- Can be caught during PCB EMC rule checking
  - For example, BoardCheck rule requires differential pair length to match


Common Mode Harmonic Growth
Fundamental Harmonic
Ratio R (CM/DM)
0.40
0.35
0.30
0.25
0.20
0.15
0.10
0.05
0.00
R(1)
TanR(1)
1st Harmonic
0.02
0.03
0.08
0.16
0.25
0.36
1
2
5
10
15
20
Normalized Skew to Bit Width (%)
Based on TUHH formula
$R = \frac{|V_{comm}|}{|V_{diff}|} = \tan\left(\frac{\beta\Delta l}{2}\right) \approx \frac{\beta\Delta l}{2}, \quad \text{if } \beta\Delta l << 1$

Example I/O Cable @ 10 Gb/s

- Fundamental Harmonic at 5 GHz
- Source = 97 dBuV
- S_{cd21} = -16 dB (from plot for 10% skew/bit-width)
- Assume cable shielding → 15 dB
- CM noise on external cable = 71 dBuV

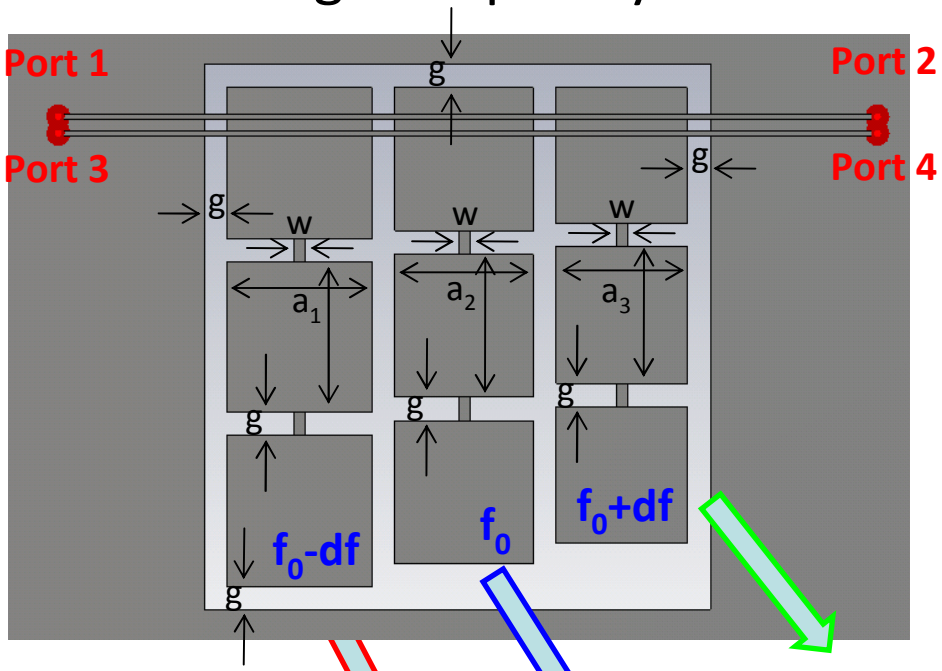
- Rule-of-thumb limit > 1 GHz = 1 mV (60 dBuV)
- CM over limit by 6 dB!

Options

- Fix skew on PCB
  - May not be possible due to routing constraints
- Improve shielding
  - Costly?
- Add filter before I/O connector
  - Discrete filters expensive and may distort intentional signal
  - Use Electromagnetic Band gap (EBG) filter?

EBG Filter Larger Bandwidth Design

Three EBG are designed to resonate around the central design frequency of 8 GHz



Courtesy of Prof Orlandi, Univ L'Aquila

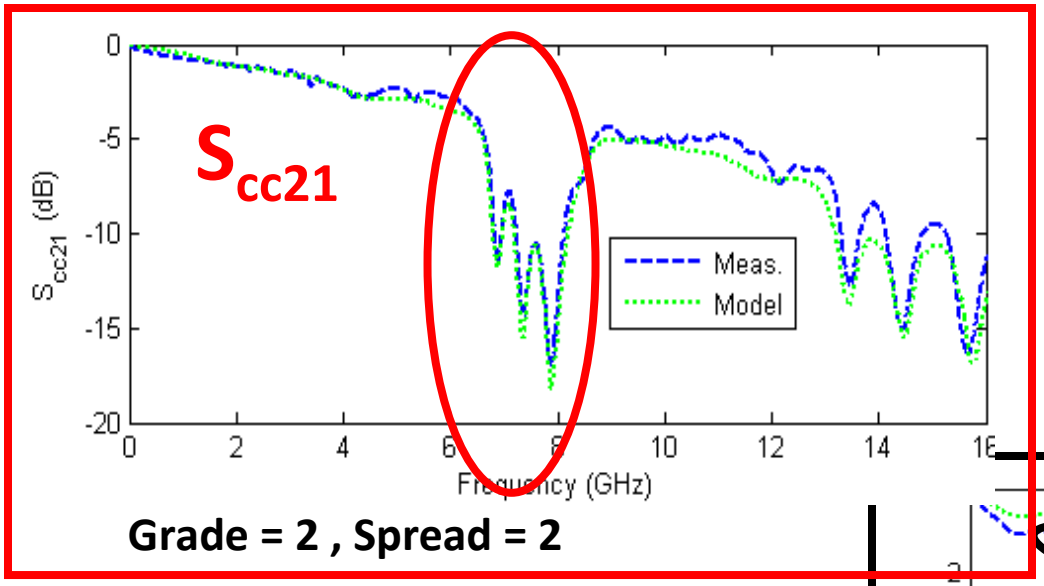
$f_{res} = f_{TM10} + 10\ \%$

$f_{res} = f_{TM10} = 8$ GHz

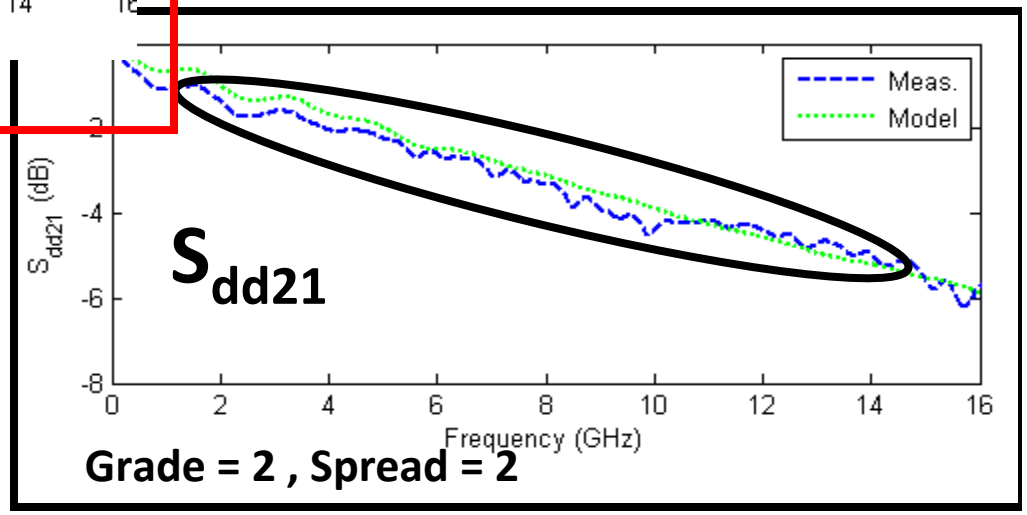
$f_{res} = f_{TM10} - 10\ \%$

Example EBG Filter Results

(Measure and Simulation Comparison)



Grade = 2 , Spread = 2

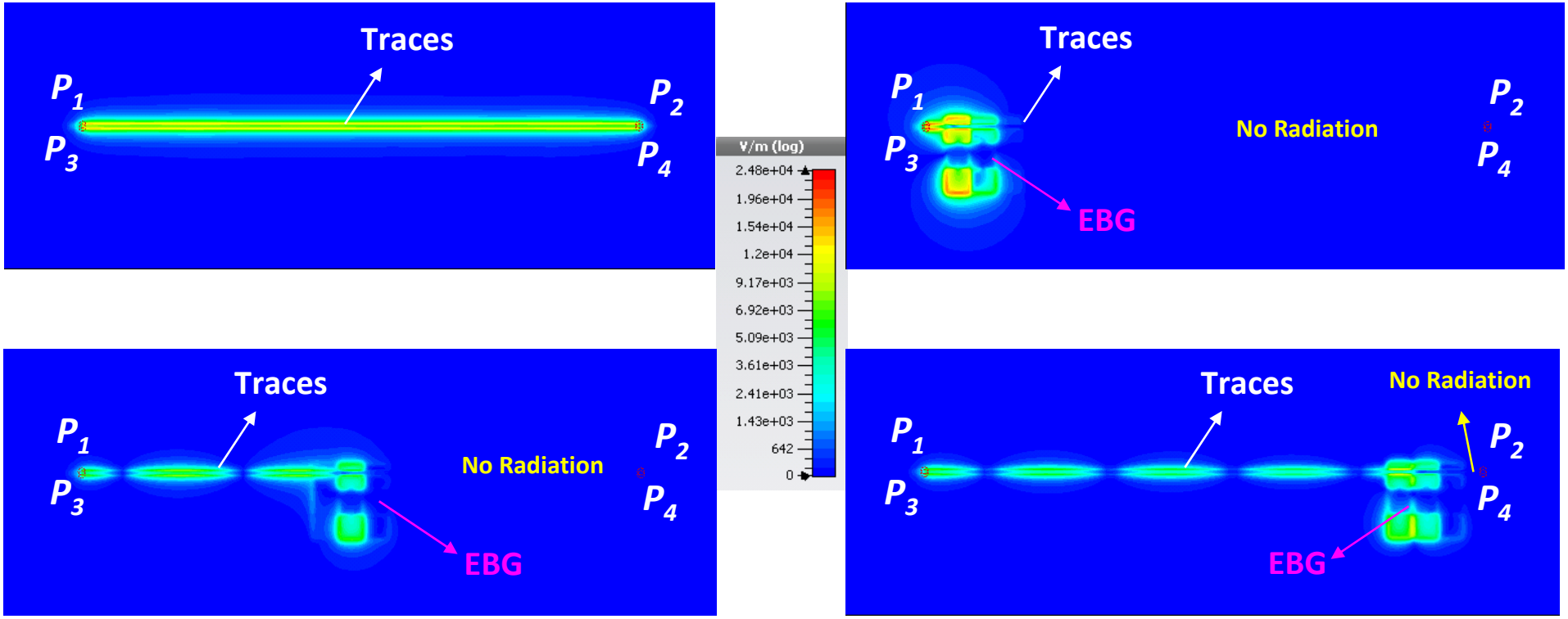


Grade = 2 , Spread = 2

Courtesy of Prof Orlandi, Univ L'Aquila

Example EBG Near Field Results

Fullwave Simulation in Microwave Studio with Different EBG Filter Locations



Courtesy of Prof Orlandi, Univ L'Aquila

SI Concerns for CM

- Some devices require CM to be below a specified amount
  - Often given in time domain
  - Beware of out-of-band CM
- S_{dc21} can convert external common mode to differential mode noise

Summary

- Many asymmetries can cause common mode noise
- When specifying the amount of CM conversion that is allowable – must include source amplitude and expected shielding
- While EMC is primary concern, SI immunity can be a consideration