Printed Circuit Board Decoupling

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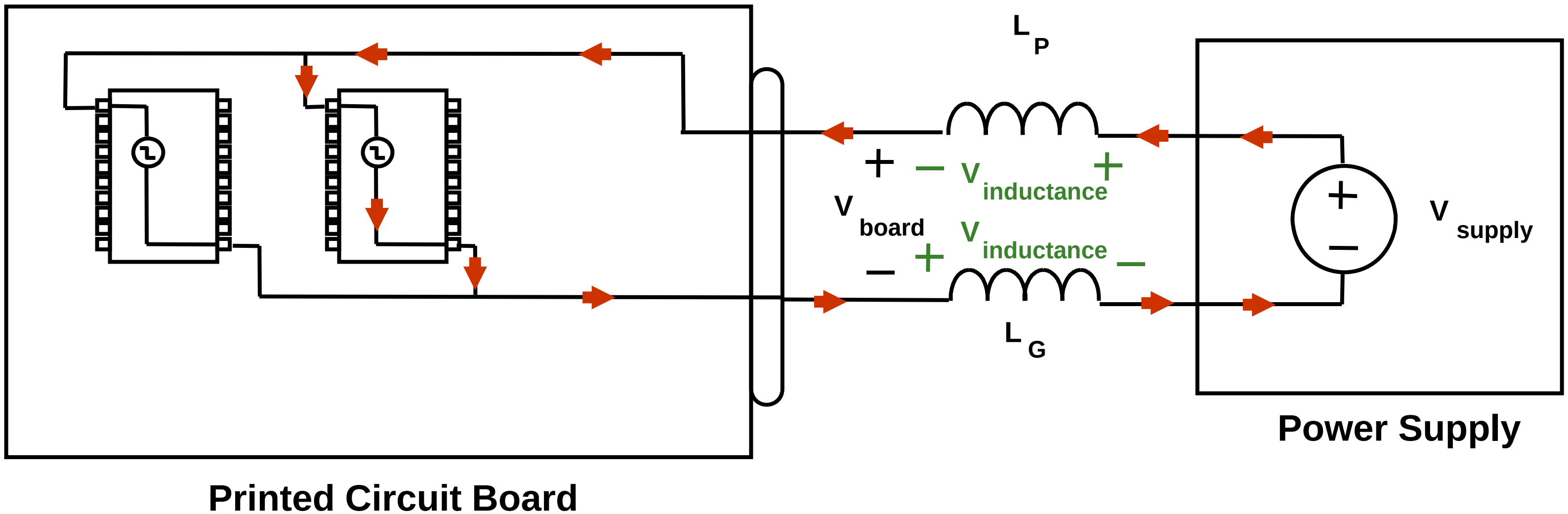
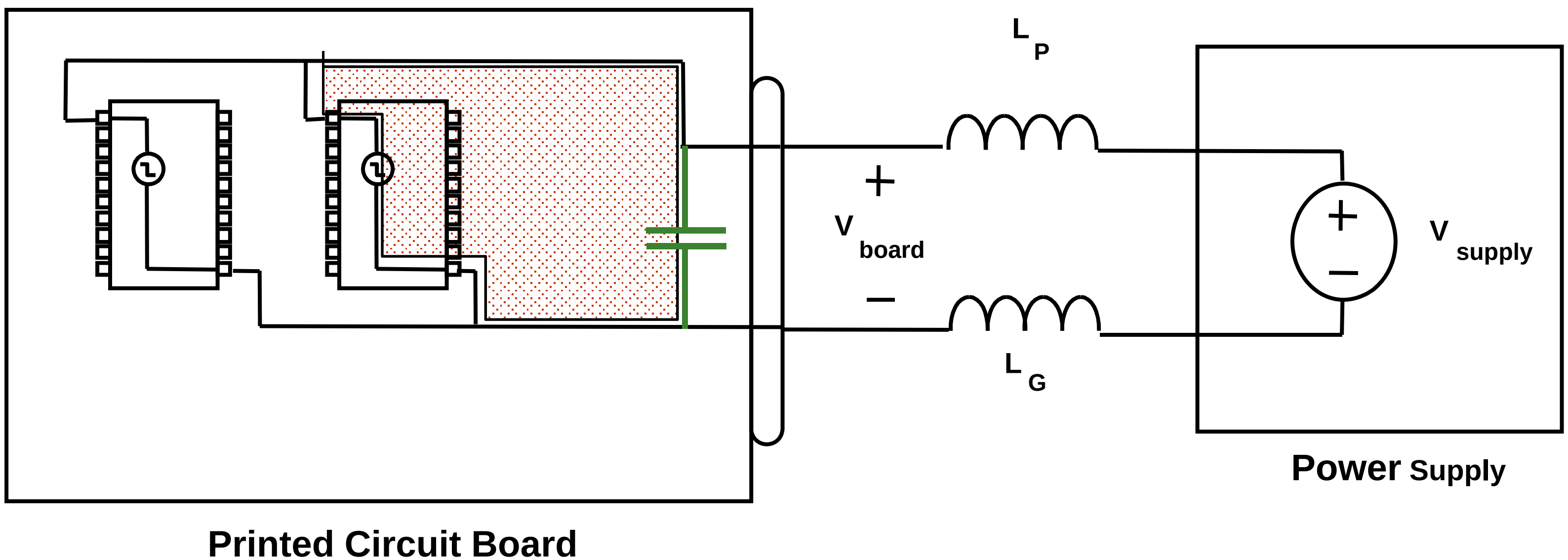
UNIVERSITY

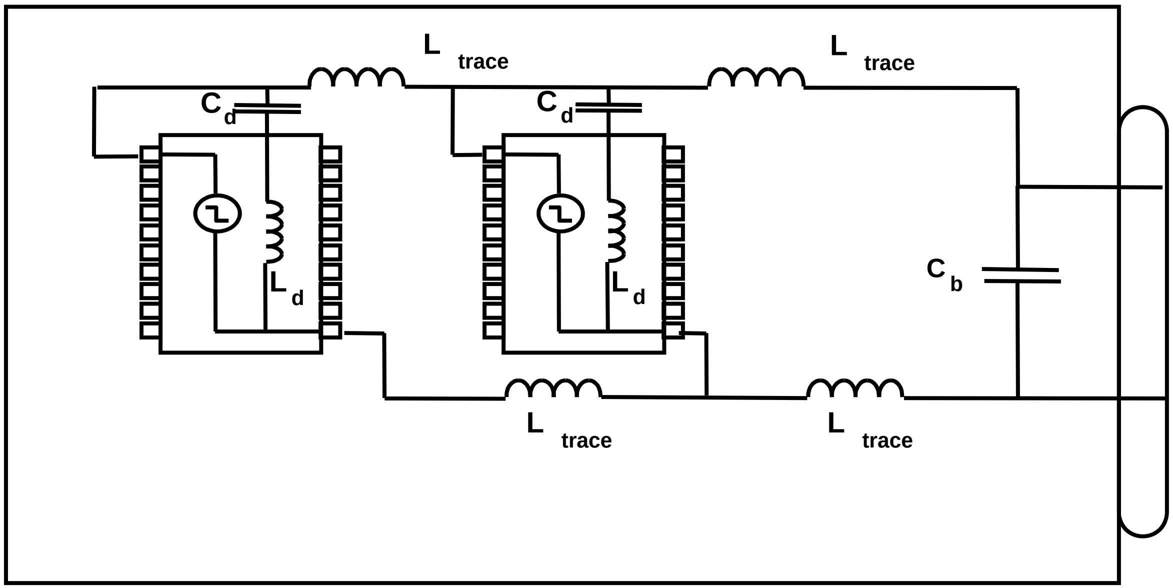
The Concept of Power Bus Decoupling



The Concept of Power Bus Decoupling



The Concept of Power Bus Decoupling

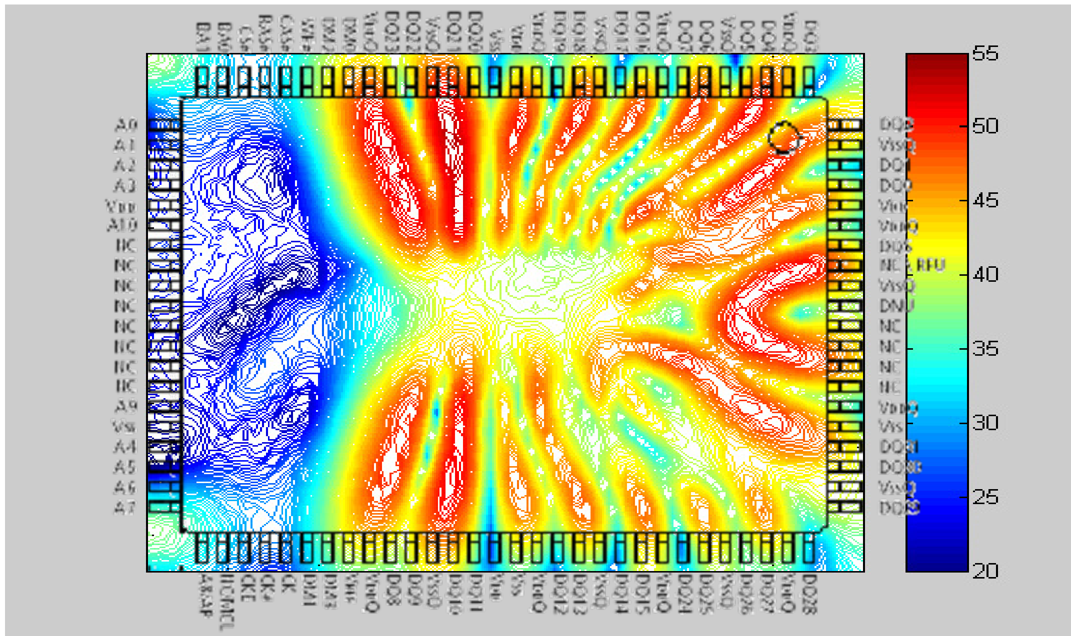


Why is this a problem?

Signal Integrity is compromised!

Power Bus Noise → Radiated and Conducted EMI!

Why is this a problem?



For some ICs, the high-frequency currents drawn from the power pins can be much greater than the high-frequency currents in the signals!

Has anybody studied this?

B. Rubin and W. D. Becker, “The Modeling of Delta-I Noise in High Performance Computer Modules,” *Conference Record of the 17th Asilomar Conference on Circuits, Systems, and Computers*, IEEE Cat. # 83CH1939-8, Oct. 31-Nov. 2, 1983.

H. W. Ott, *Noise Reduction Techniques in Electronic Systems, 2nd Ed.*, John Wiley Interscience, New York, 1988.

N. Raver et al., “Circuit Noise Study,” *Proceedings of the technical program for NEPCON WEST 92*, Anaheim Convention Center, Anaheim CA, pp. 77-86, Feb. 23-27, 1992.

R. Downing, P. Gebler, G. Katopis, “Decoupling Capacitor Effects on Switching Noise,” *Conference Record of the IEEE Topical Meeting on Electrical Performance of Electronic Packaging*, IEEE Cat. # 92TH0452-5, Apr. 22-24, 1992.

A. R. Djordjevic and T. K. Sarkar, “An Investigation of Delta-I Noise on Integrated Circuits,” *IEEE Trans. on Electromagnetic Compat.*, vol. 35, no. 2, May 1993.

J. Sisler, “Eliminating Capacitors From Multilayer PCBs,” Printed Circuit Design, July 1991.

C. Dirks, “Wideband Supply Voltage Decoupling for Integrated Circuits,” EMC Test & Design, November/December, 1992.

T. Wang, “Characteristics of Buried Capacitance,” EMC

S. Daijavad and H. Heeb, “On the Effectiveness of Dec
Proc. Of the IEEE EMC Symposium, Atlanta, GA

T. H. Hubing, J. L. Drewniak, T. P. Van Doren, and D. Hockanson, “Power Bus Decoupling on Multilayer Printed Circuit Boards,” *IEEE Transactions on Electromagnetic Compatibility*, vol. EMC-37, no. 2, May 1995, pp. 155-166.

H. Shi, F. Sha, J. L. Drewniak, T. H. Hubing, T. P. Van Doren, and F. Yuan, "Simulation and Measurement for Decoupling on Multilayer PCB DC Power Buses," *Proceedings of the 1996 IEEE International Symposium on Electromagnetic Compatibility,* Santa Clara, CA, August 1996, pp. 430-435.

A lot of people have been looking at the power bus noise problem for a long time.

John R. Barnes’ Bibliography has 837 entries.

Conflicting Rules for PCB Decoupling

Use small-valued capacitors for high-frequency decoupling.

Locate capacitors near the power pins of active devices.

Use 0.01 μF for local decoupling!

Use capacitors with a low ESR!

Avoid capacitors with a low ESR!

Use 0.001 μF for local decoupling!

Locate capacitors near the ground pins of active devices.

Run traces from device to capacitor, then to power planes.

Location of decoupling capacitors is not relevant.

Never put traces on decoupling capacitors.

Use the largest valued capacitors you can find in a given package size.

Local decoupling capacitors should have a range of values from 100 pF to 1 μF!

Main Questions

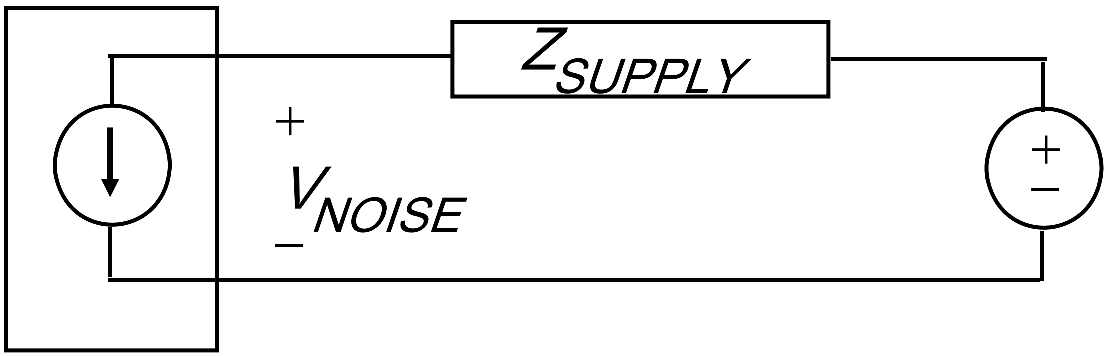
- How much capacitance do I need?
- Where should it be located?
- How should it be connected?

Conflicting Goals?

- **Do we want a low-impedance power bus that can supply lots of current without a significant change in voltage?**

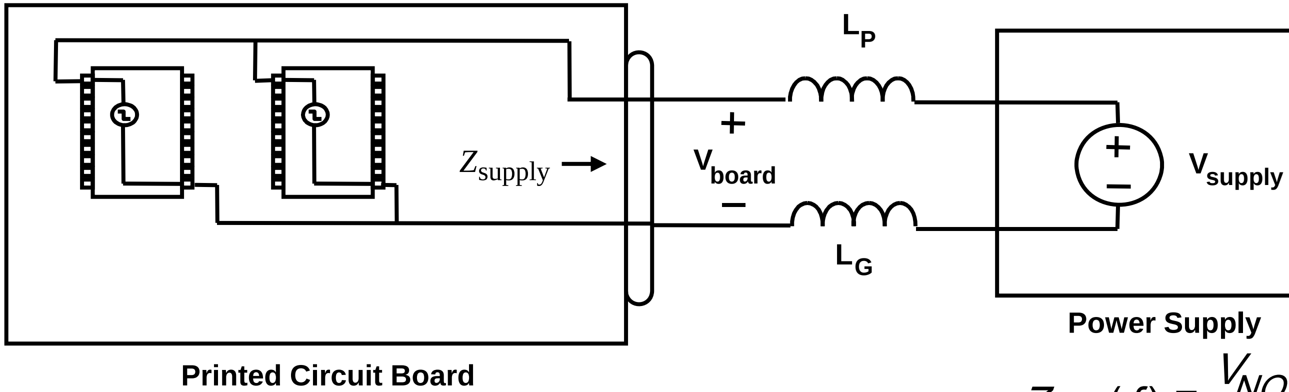
- **Do we want a high-impedance power bus that isolates each device from other devices?**

How much capacitance do you need?

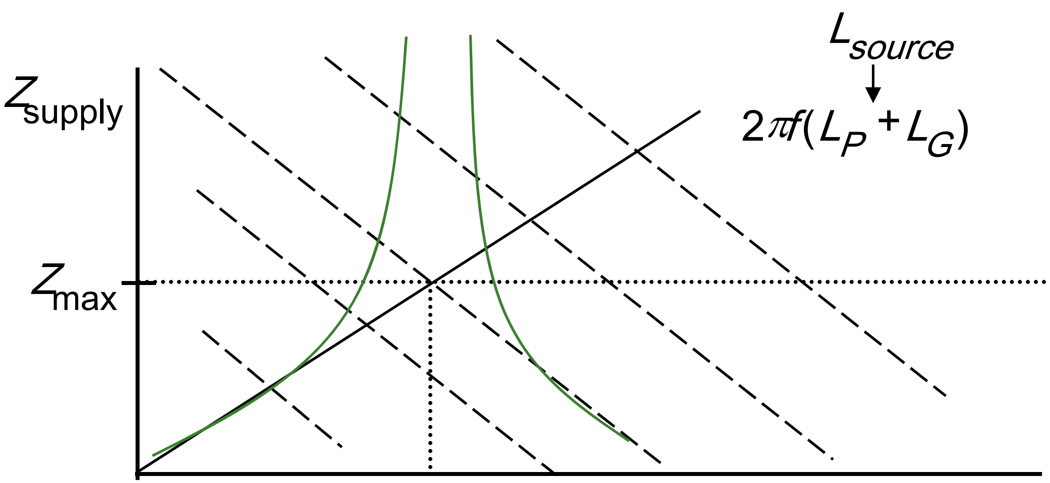


$$V_{NOISE} = Z_{SUPPLY} I_{DEVICE}$$

How much capacitance do you need?



$$Z_{max}(f) = \frac{V_{NOISEMAX}(f)}{I_{DEVICEMAX}(f)}$$



$$f_0 = \frac{Z_{max}}{2\pi L_{source}}$$

$$\frac{1}{2\pi f_0 C} = Z_{max}$$

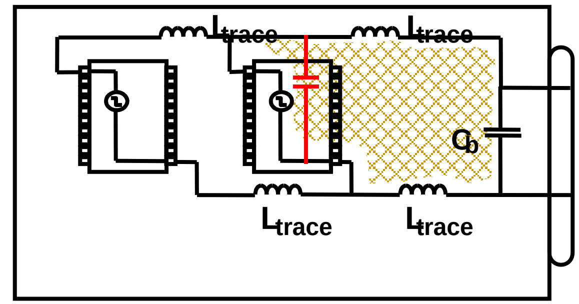
$$C_{min} = \frac{1}{2\pi f_0 Z_{max}}$$

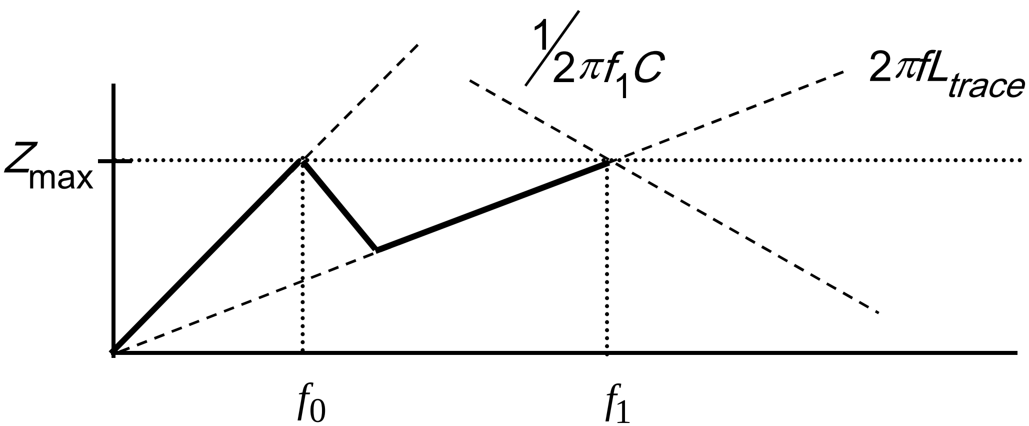
$$= \frac{1}{(2\pi f_0)^2 L_{source}}$$

How much capacitance do you need?

Impedance approach

$$Z_{max}(f) = \frac{V_{NOISEMAX}(f)}{I_{DEVICEMAX}(f)}$$





$$\frac{1}{2\pi f_0 C} = Z_{max}$$

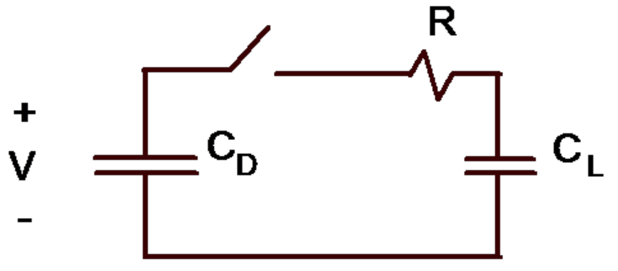
$$C_{min} = \frac{1}{2\pi f_0 Z_{max}}$$

$$= \frac{1}{(2\pi f_0)^2 L_{source}}$$

How much capacitance do you need?

Capacitance Ratio approach

Recognizing that CMOS loads are capacitances, we are simply using decoupling capacitors to charge load capacitances.

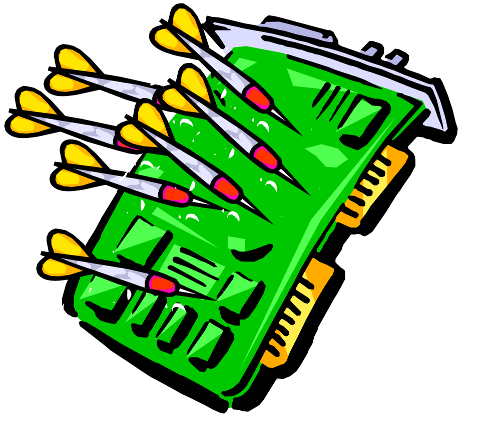


Total decoupling capacitance is set to a value that is equal to the total device capacitance times the power bus voltage divided by the maximum power bus noise.

How much capacitance do you need?

Guidelines approach

Let's do it the way that worked for somebody at sometime in the past.



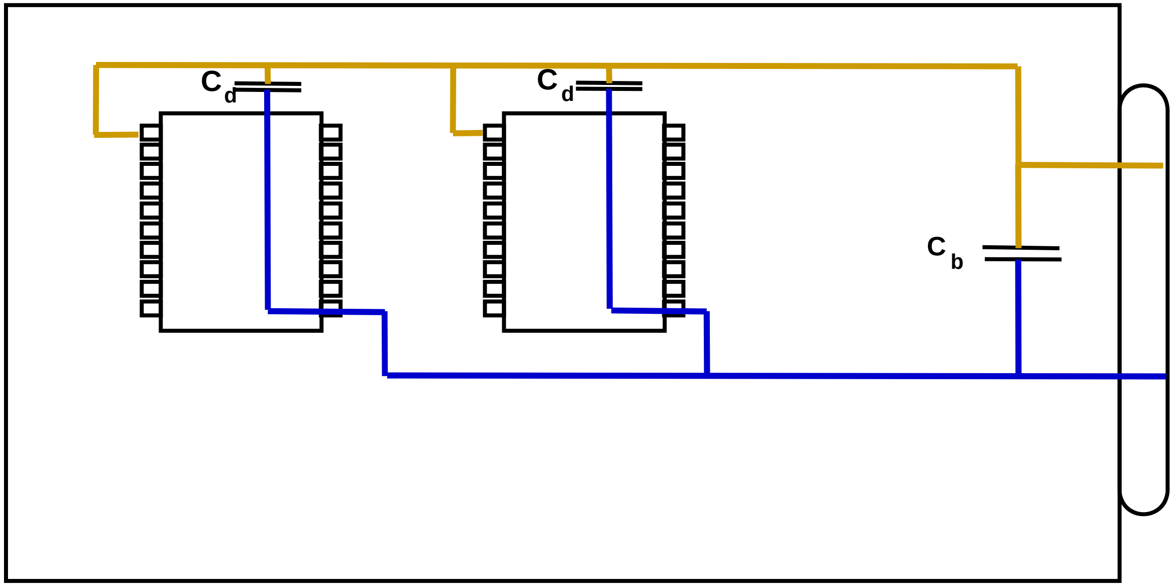
"… include one 0.01 uF local decoupling capacitor for each VCC pin of every active component on the board plus 1 bulk decoupling capacitor with a value equal to 5 times the sum of the local decoupling capacitance." .

Main Questions

- ☑ How much capacitance do I need?
- ☐ Where should it be located?
- ☐ How should it be connected?

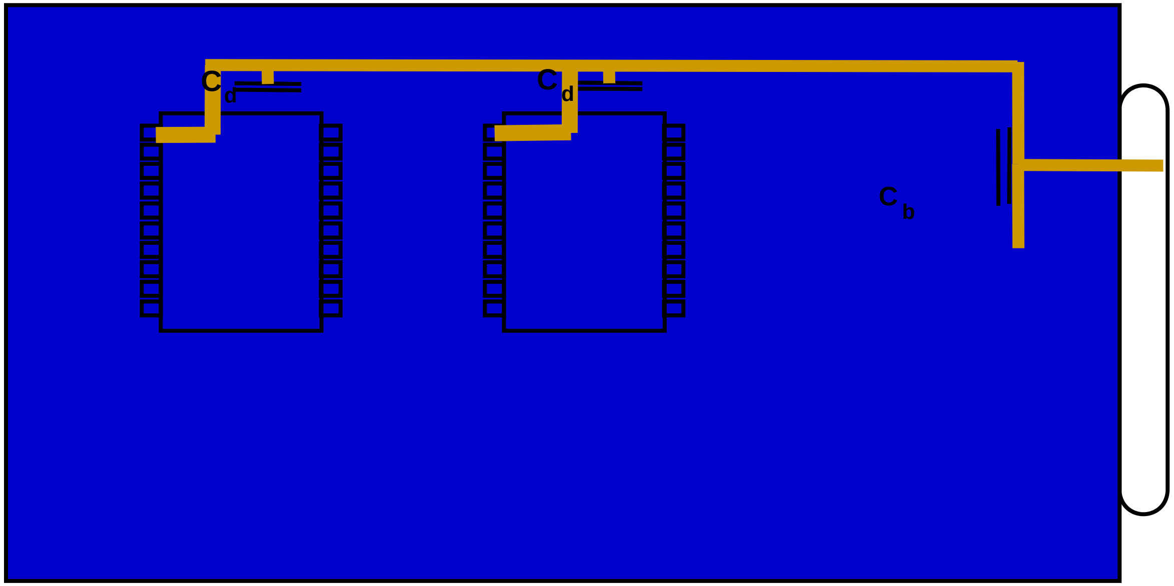
Printed Circuit Board Decoupling Strategies

Boards without Power Planes



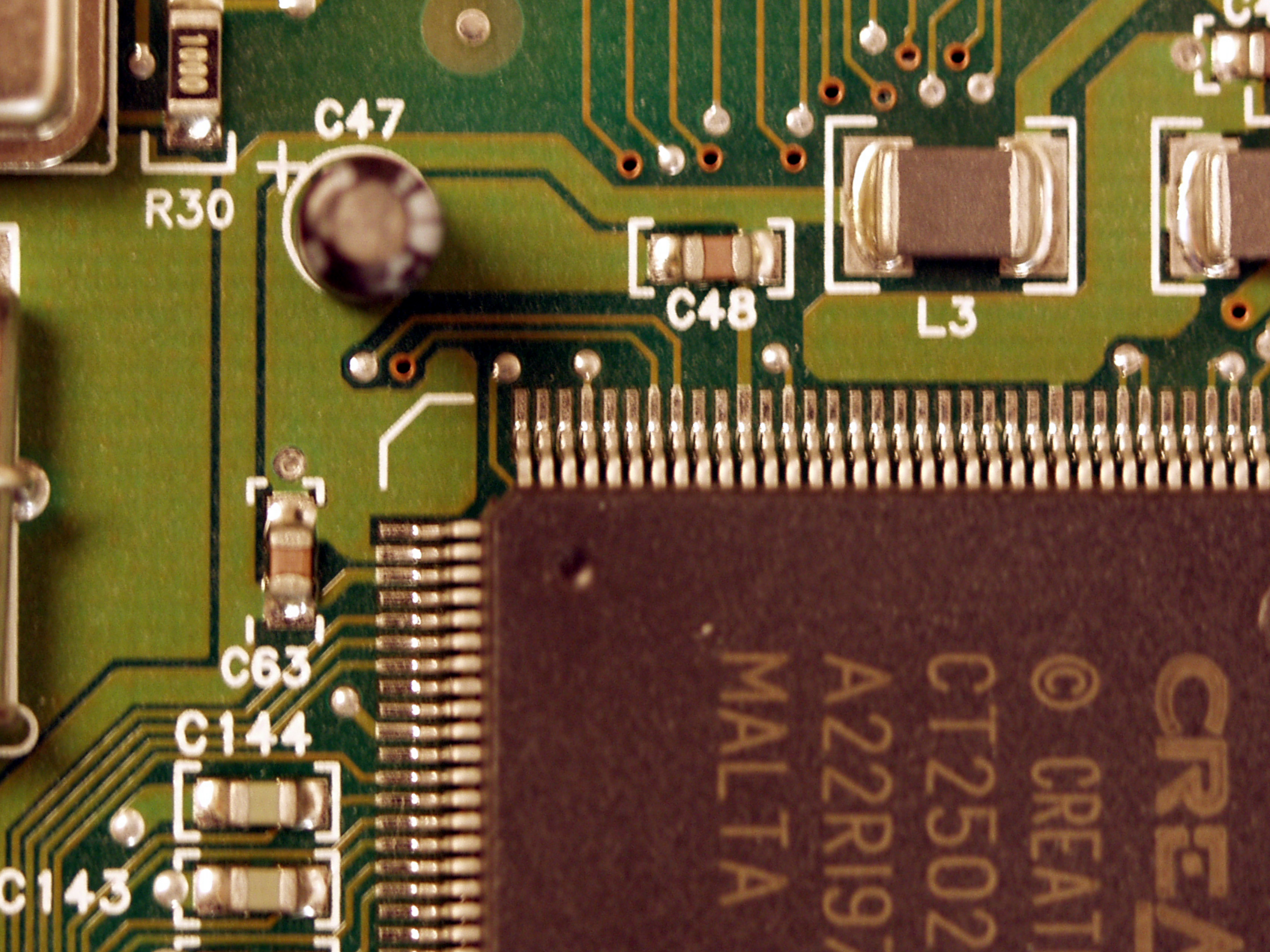
OK?

Boards without Power Planes



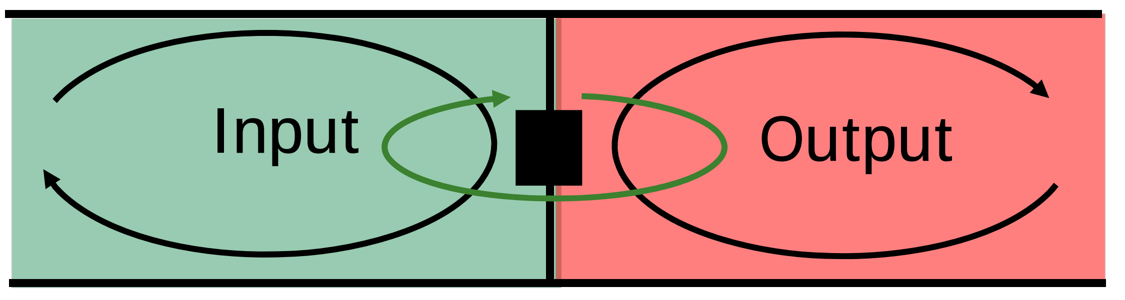
Got a ground plane?


9A472J
2K
C117
L8
C129
R66
7C26
LS245
C128
R68
R70
C140
U17
L9
1R0
NOLOGY LTD 1995

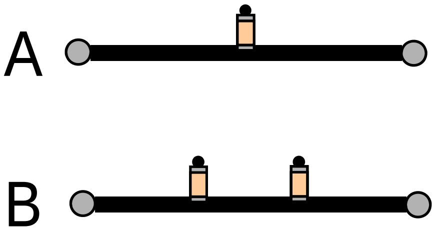

C47
R30
C48
L3
C63
C144
C143
MALTA

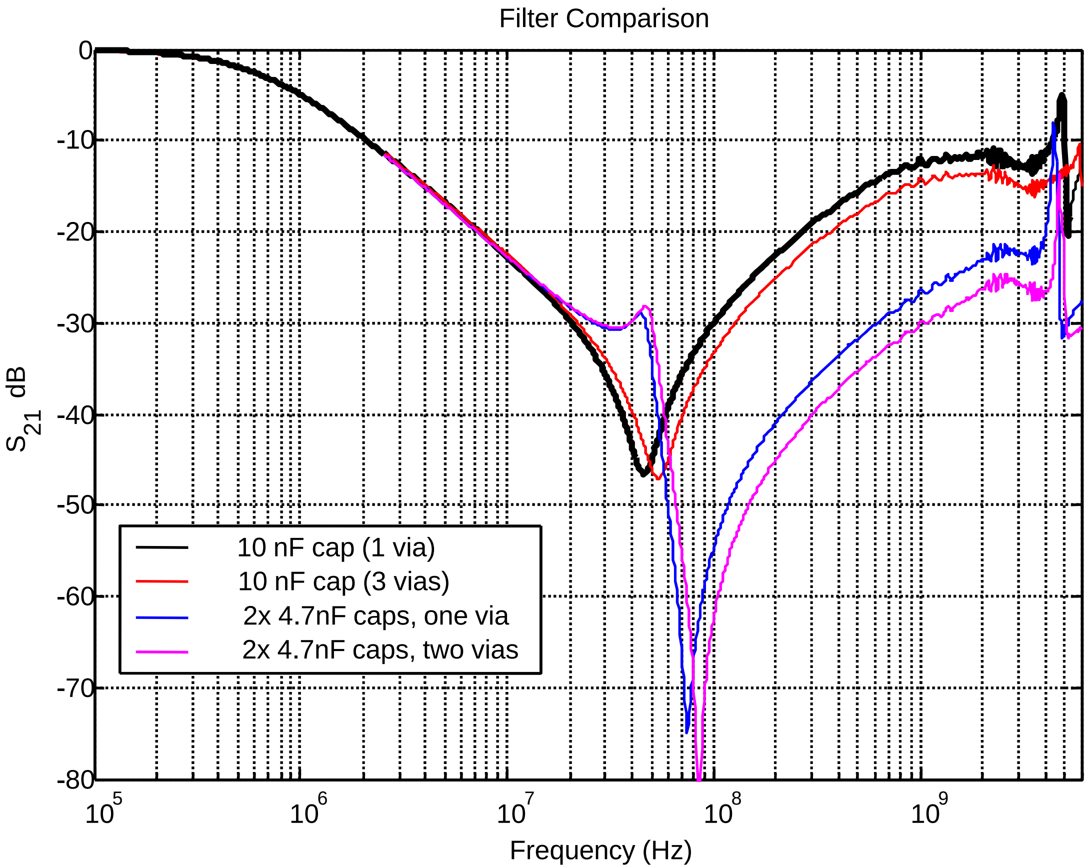
Boards without Power Planes

The effectiveness of a single capacitor as a filter is limited by mutual inductance.



Boards without Power Planes





Two capacitors can be much more effective than one.

Power Bus Decoupling Strategy

With no power plane

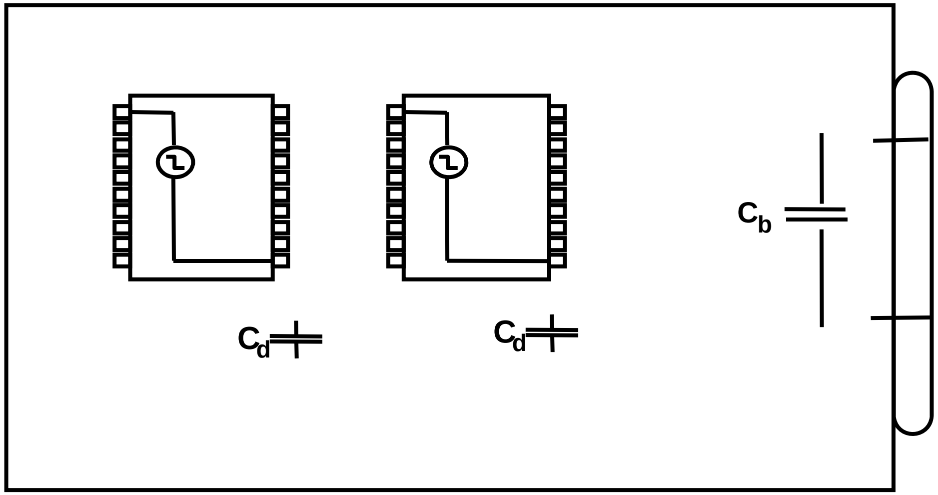
- **layout low-inductance power distribution**
- **size bulk decoupling to meet board requirements**
- **size local decoupling to meet device requirements**
- **two caps can be much better than one**
- **avoid resonances by minimizing L**

References:

T. Hubing, "Printed Circuit Board Power Bus Decoupling," *LG Journal of Production Engineering*, vol. 3, no. 12, December 2000, pp. 17-20. (Korean language publication) .

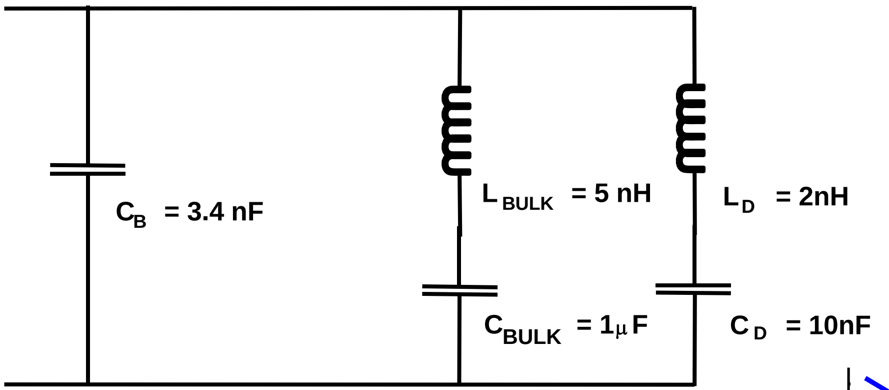
T. Zeeff, T. Hubing, T. Van Doren and D. Pommerenke, "Analysis of simple two-capacitor low-pass filters," IEEE Transactions on Electromagnetic Compatibility, vol. 45, no. 4, Nov. 2003, pp. 595-601.

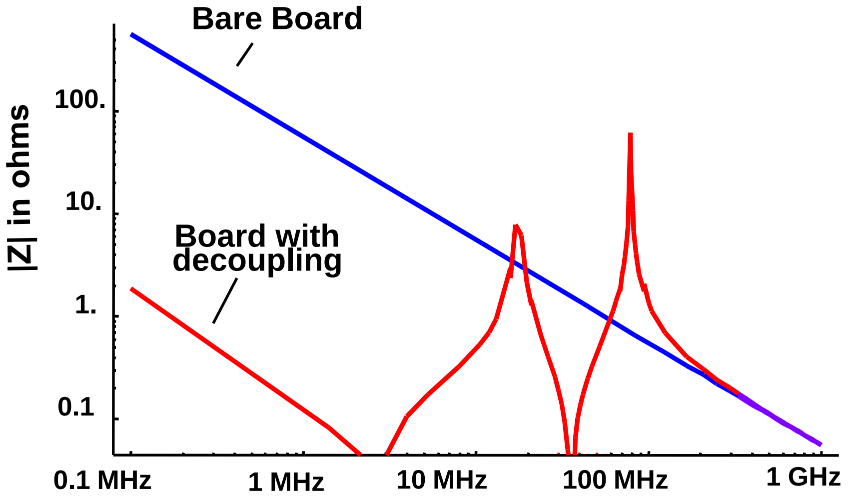
Boards with Closely Spaced Power Planes



Power Distribution Model ~ (5 - 500 MHz)
Board with power and ground planes

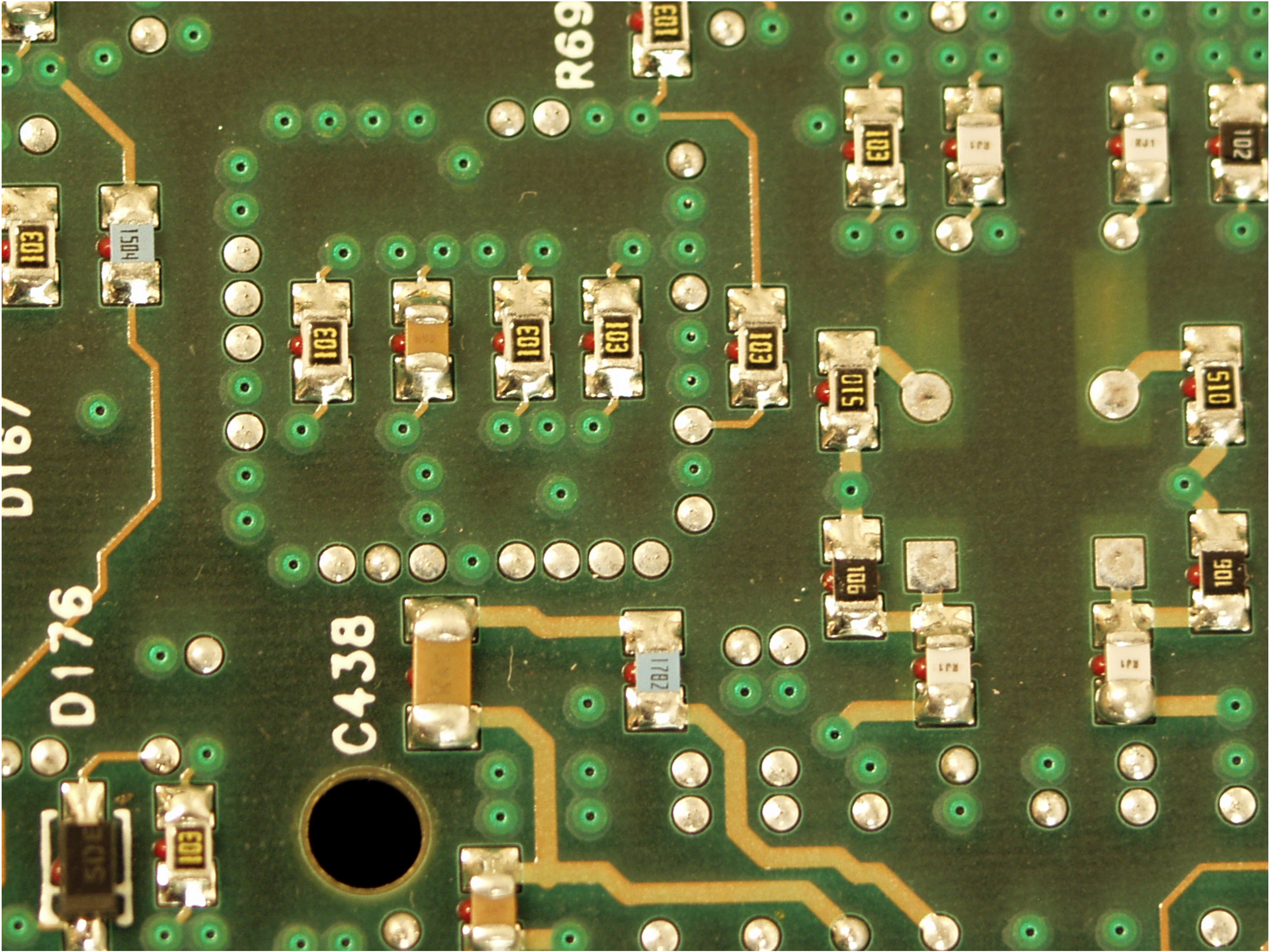
Boards with Closely Spaced Power Planes





For Boards with "Closely-Spaced" Planes

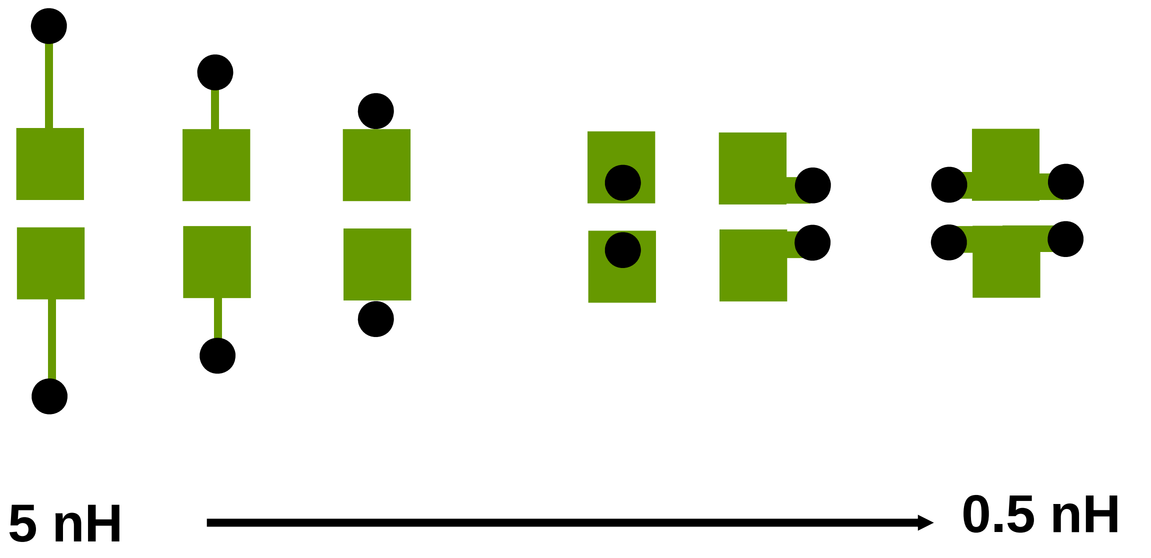
- The location of the decoupling capacitors is not critical.
- The value of the local decoupling capacitors is not critical, but it must be greater than the interplane capacitance.
- The inductance of the connection is the most important parameter of a local decoupling capacitor.
- None of the local decoupling capacitors are effective above a couple hundred megahertz.
- None of the local decoupling capacitors are supplying significant charge in the first few nanoseconds of a transition.


R69
C438
D176
103
510
106
102

Inductance of connections to planes

On boards with closely spaced power and ground planes:

Generally speaking, 100 decoupling capacitors connected through 1 nH of inductance will be as effective as 500 decoupling capacitors connected through 5 nH of inductance.



Power Bus Decoupling Strategy

With closely spaced (<.25 mm) planes

- **size bulk decoupling to meet board requirements**
- **size local decoupling to meet board requirements**
- **mount local decoupling in most convenient locations**
- **don’t put traces on capacitor pads**
- **too much capacitance is ok**
- **too much inductance is not ok**

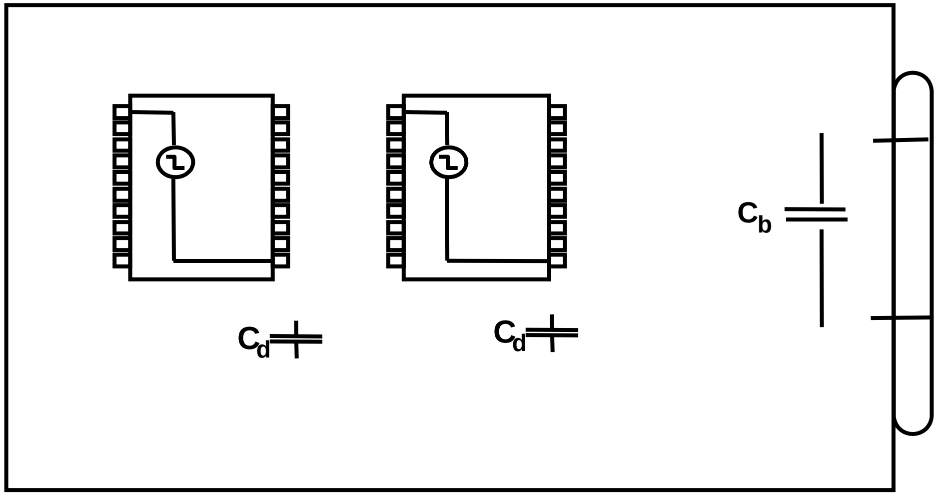
References:

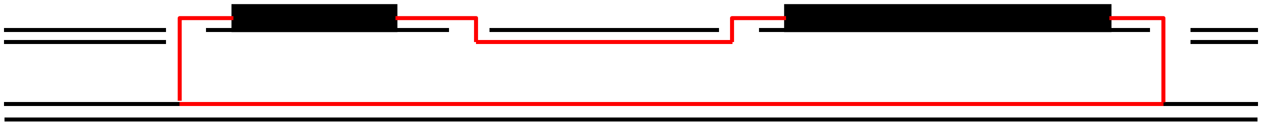
T. H. Hubing, J. L. Drewniak, T. P. Van Doren, and D. Hockanson, “Power Bus Decoupling on Multilayer Printed Circuit Boards,” *IEEE Transactions on Electromagnetic Compatibility*, vol. EMC-37, no. 2, May 1995, pp. 155-166.

T. Zeeff and T. Hubing, “Reducing power bus impedance at resonance with lossy components,” IEEE Transactions on Advanced Packaging, vol. 25, no. 2, May 2002, pp. 307-310.

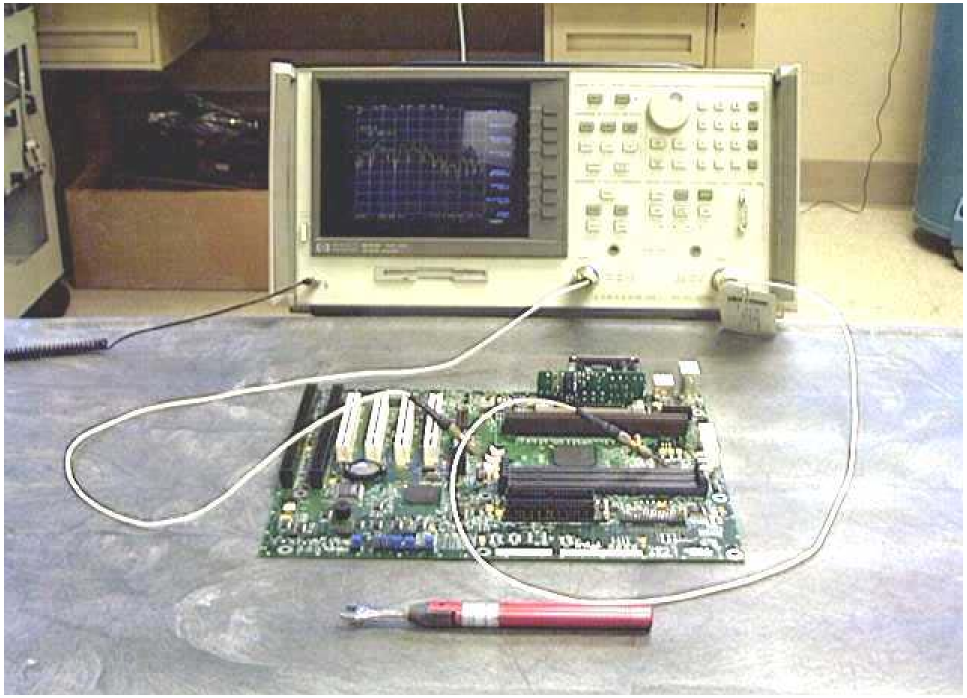
M. Xu, T. Hubing, J. Chen, T. Van Doren, J. Drewniak and R. DuBroff, “Power bus decoupling with embedded capacitance in printed circuit board design,” IEEE Transactions on Electromagnetic Compatibility, vol. 45, no. 1, Feb. 2003, pp. 22-30.

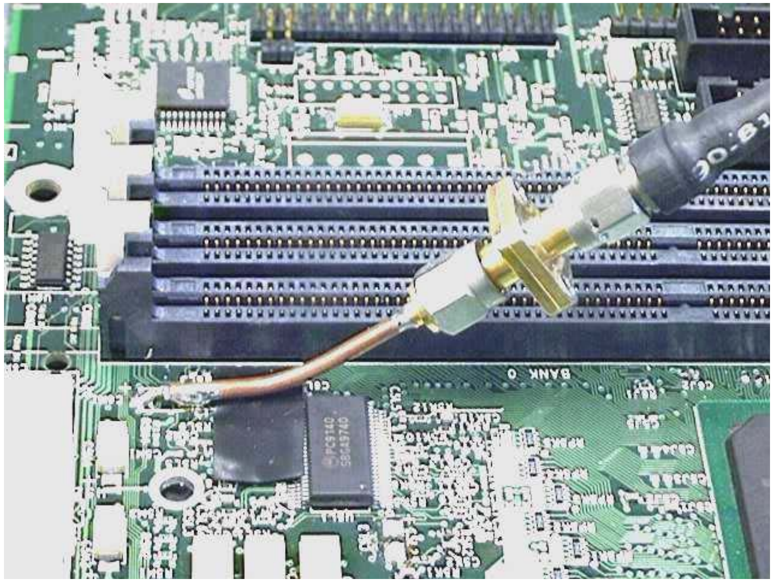
Boards with Power Planes Spaced >0.5 mm



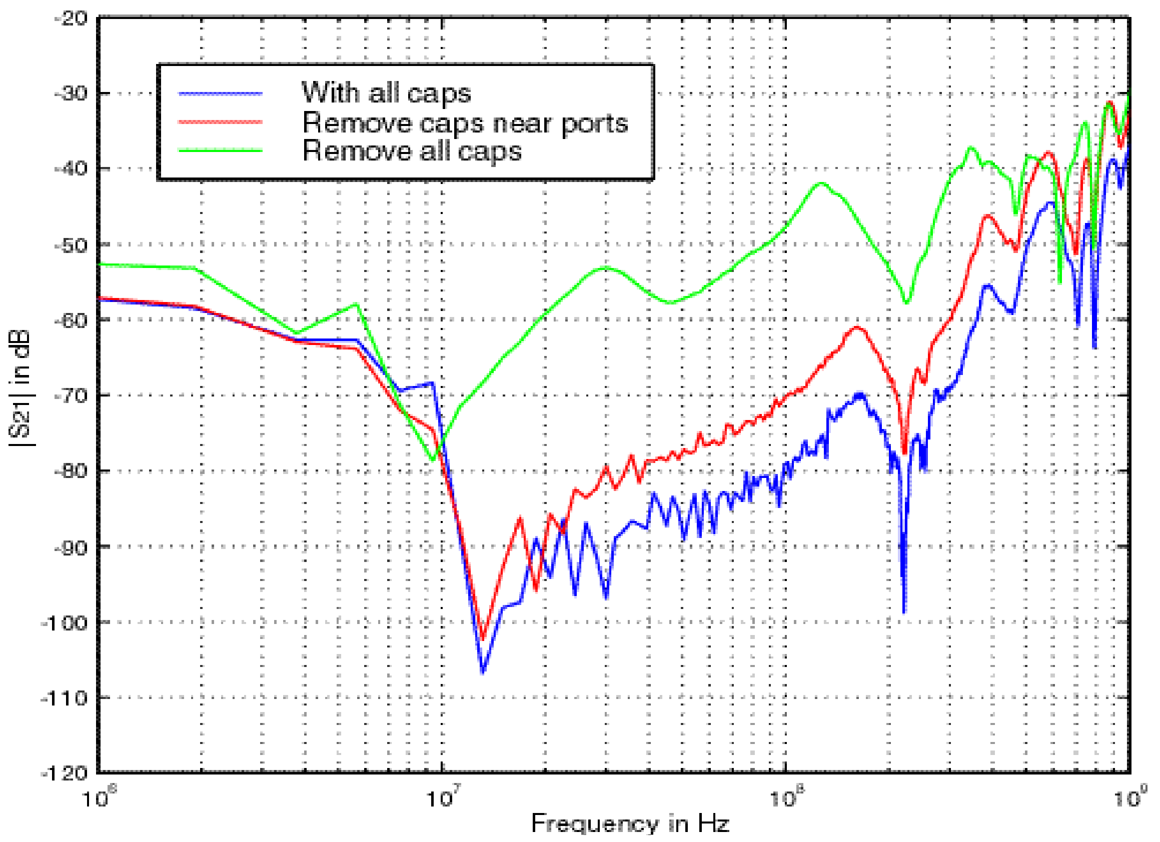


4-Layer Board Measurements

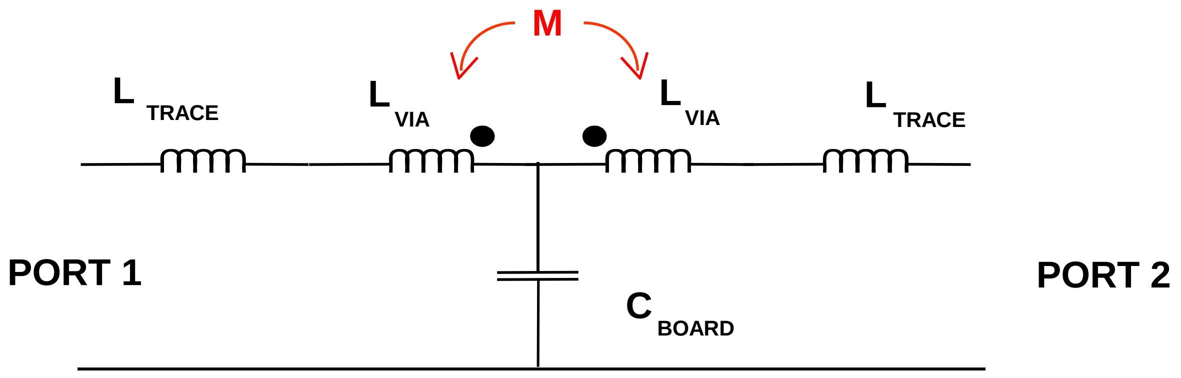


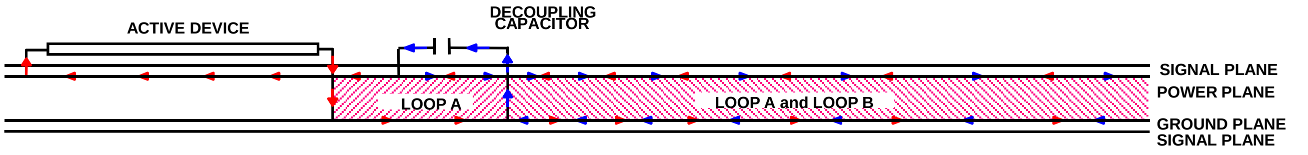


4-Layer Board Measurements



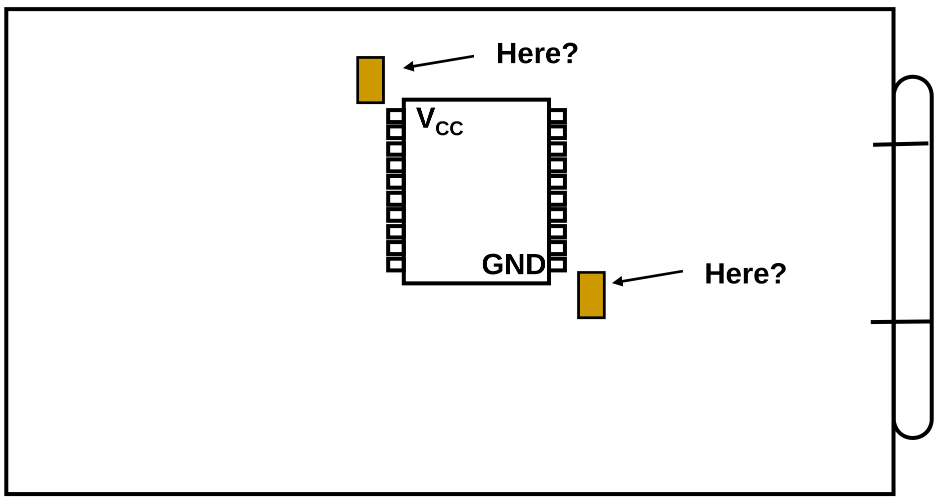
Boards with Power Planes Spaced >0.5 mm

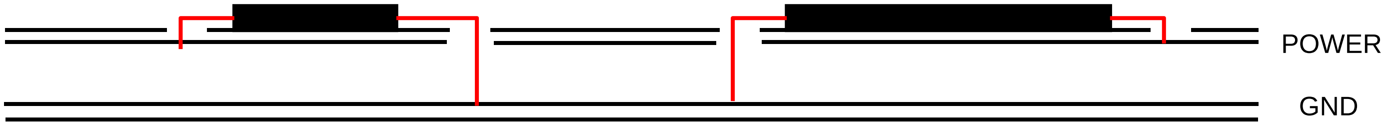




On boards with a spacing between power and ground planes of ~30 mils (0.75 mm) or more, the inductance of the planes can no longer be neglected. In particular, the mutual inductance between the vias of the active device and the vias of the decoupling capacitor is important. The mutual inductance will tend to cause the majority of the current to be drawn from the nearest decoupling capacitor and not from the planes.

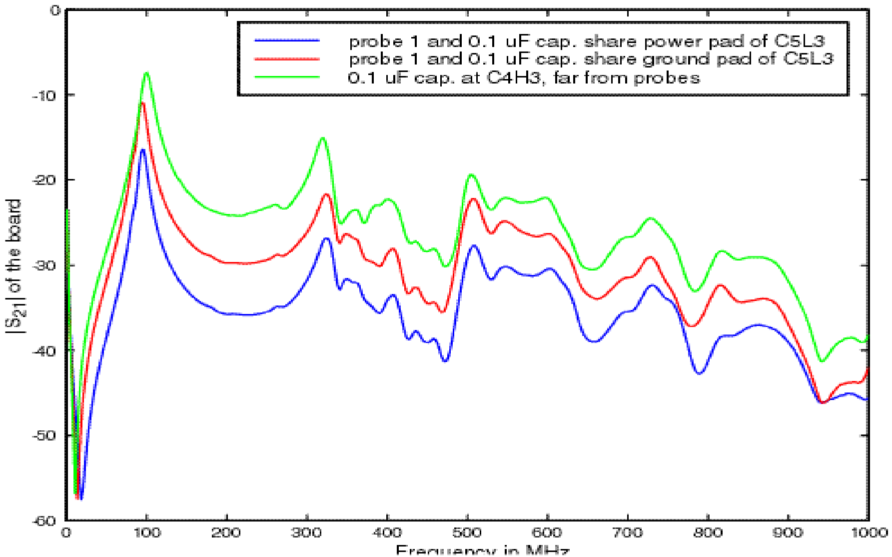
Where do I mount the capacitor?

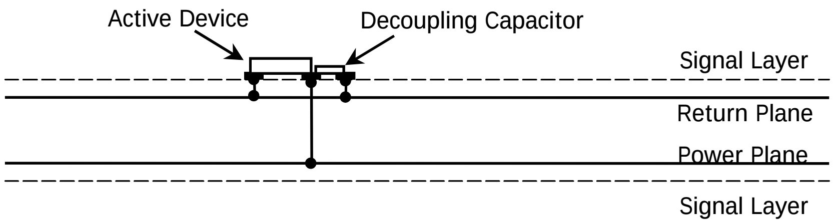


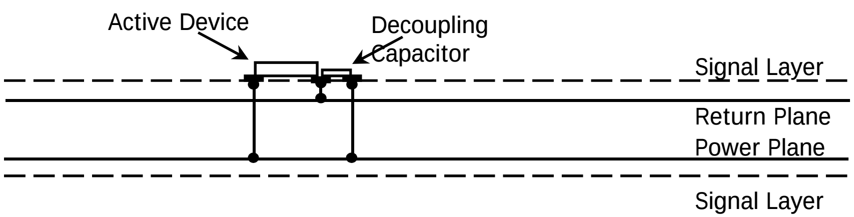


4-Layer Board Measurements

$|S_{21}|$ With Capacitor Sharing One Pad With Port 1







SMC
FDC37C677
A9731-A54910
6C7727.1
©PHOENIX 1995 MK42
U7B1
C7B1
RP7C1
RP7C2
RP7C6
C7C1
C7C2
R7C3
R7C1
R7C2
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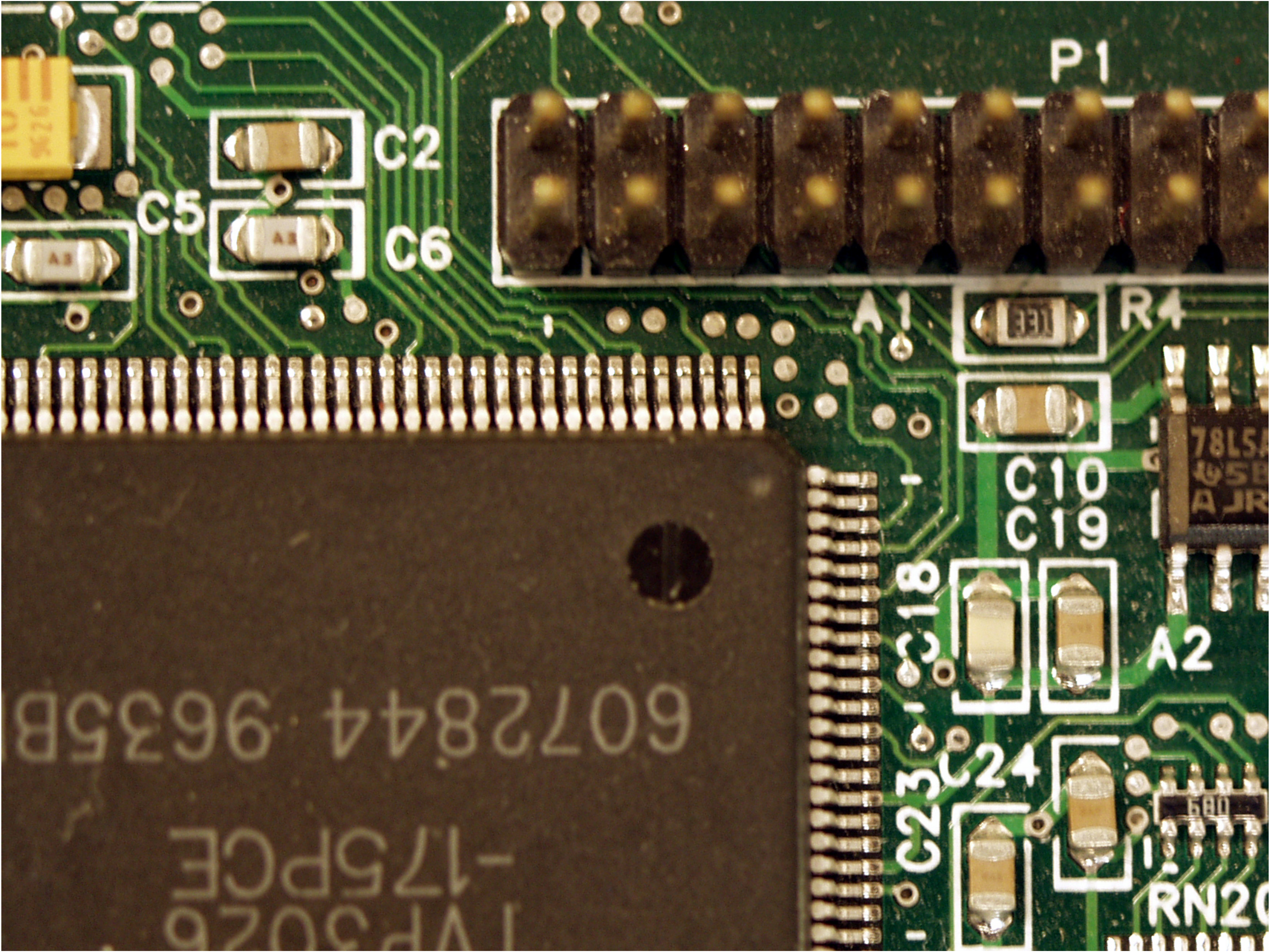
R7B2
U8C1


P1
C2
C5
C6
A1
R4
C10
C19
C18
A2
C23
C24
TVP3026
-175PCE
6072844

For Boards with “Widely-Spaced” Planes

- Local decoupling capacitors should be located as close to the active device as possible (near pin attached to most distant plane).
- The value of the local decoupling capacitors should be 10,000 pF or greater.
- The inductance of the connection is the most important parameter of a local decoupling capacitor.
- Local decoupling capacitors can be effective up to 1 GHz or higher if they are connected properly.

Power Bus Decoupling Strategy

With widely spaced (>.5 mm) planes

- **size bulk decoupling to meet board requirements**
- **size local decoupling to meet device requirements**
- **mount local decoupling near pin connected to furthest plane**
- **don't put traces on capacitor pads**
- **too much capacitance is ok**
- **too much inductance is not ok**

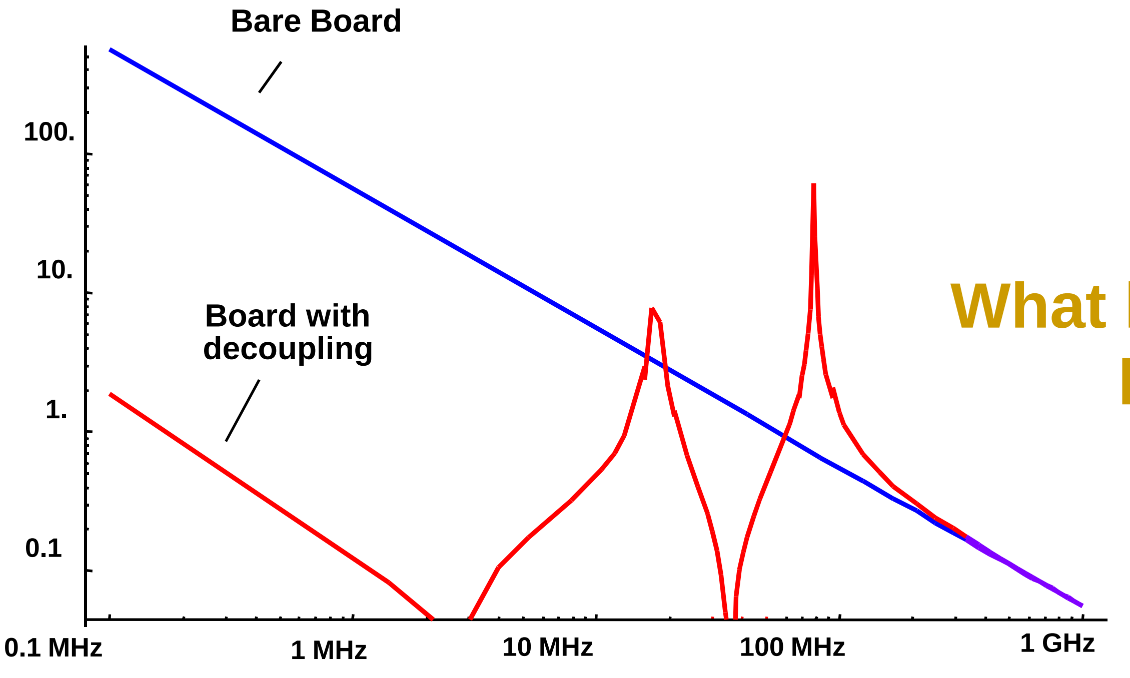
References:

J. Chen, M. Xu, T. Hubing, J. Drewniak, T. Van Doren, and R. DuBroff, "Experimental evaluation of power bus decoupling on a 4-layer printed circuit board," *Proc. of the 2000 IEEE International Symposium on Electromagnetic Compatibility*, Washington D.C., August 2000, pp. 335-338.

T. H. Hubing, T. P. Van Doren, F. Sha, J. L. Drewniak, and M. Wilhelm, "An Experimental Investigation of 4-Layer Printed Circuit Board Decoupling," *Proceedings of the 1995 IEEE International Symposium on Electromagnetic Compatibility,* Atlanta, GA, August 1995, pp. 308-312.

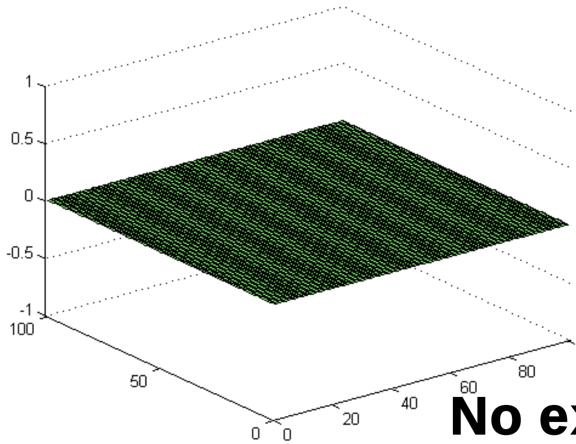
J. Fan, J. Drewniak, J. Knighten, N. Smith, A. Orlandi, T. Van Doren, T. Hubing and R. DuBroff, "Quantifying SMT Decoupling Capacitor Placement in DC Power-Bus Design for Multilayer PCBs," IEEE Transactions on Electromagnetic Compatibility, vol. EMC-43, no. 4, Nov. 2001, pp. 588-599.

Power Bus Resonances

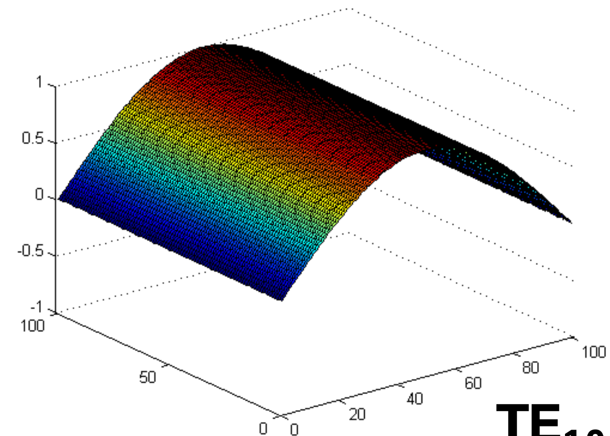


What happens here?

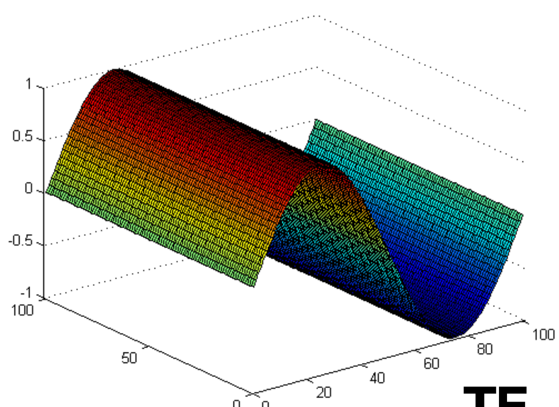
Power Bus Resonances



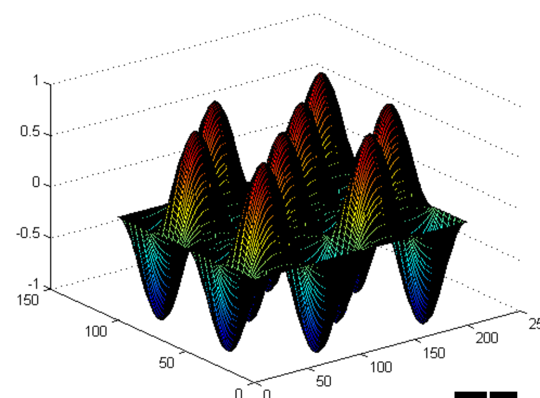
No excitation



TE_{10}



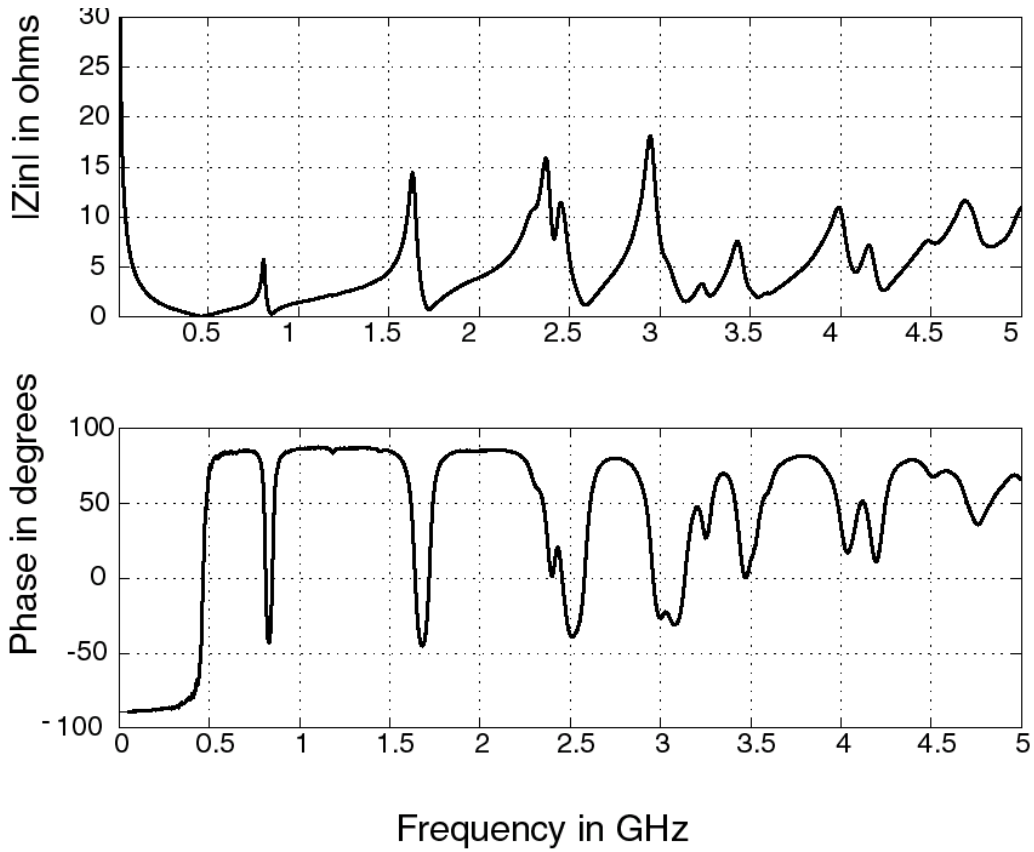
TE_{20}



TE_{44}

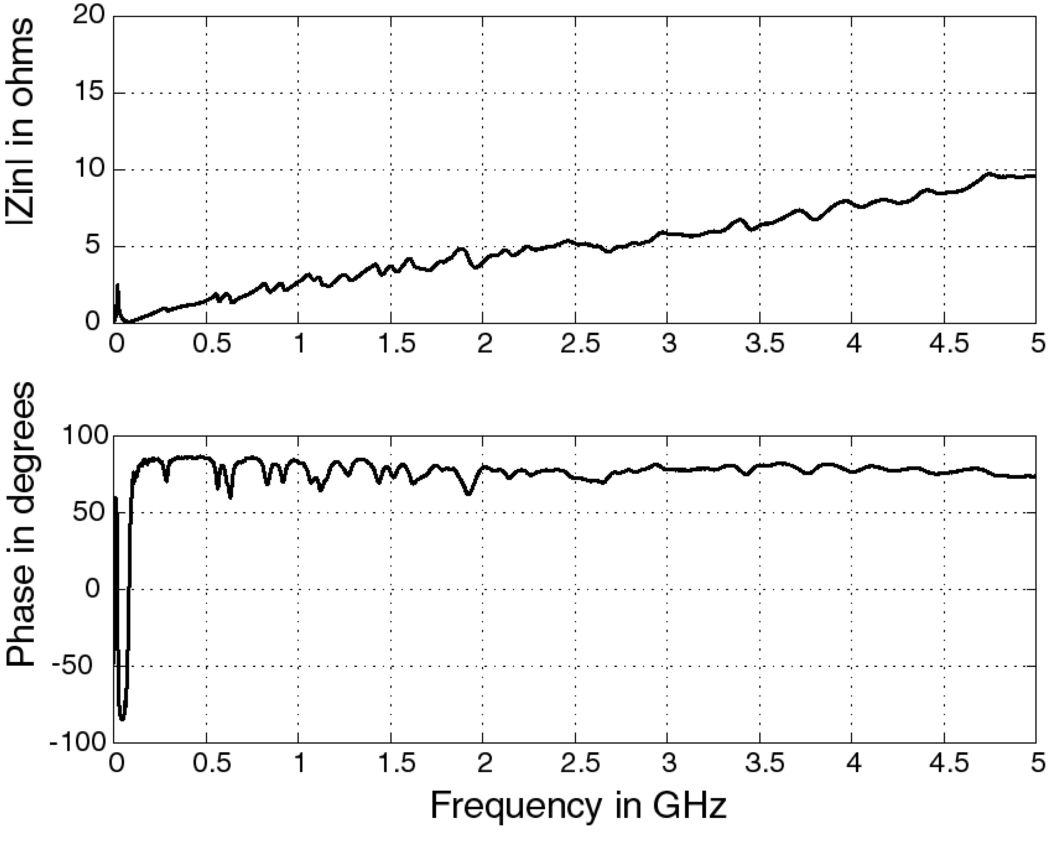
Power Bus Resonances

Input impedance of an unpopulated 2” x 3” FR4 board with 22-mil power/ground plane spacing



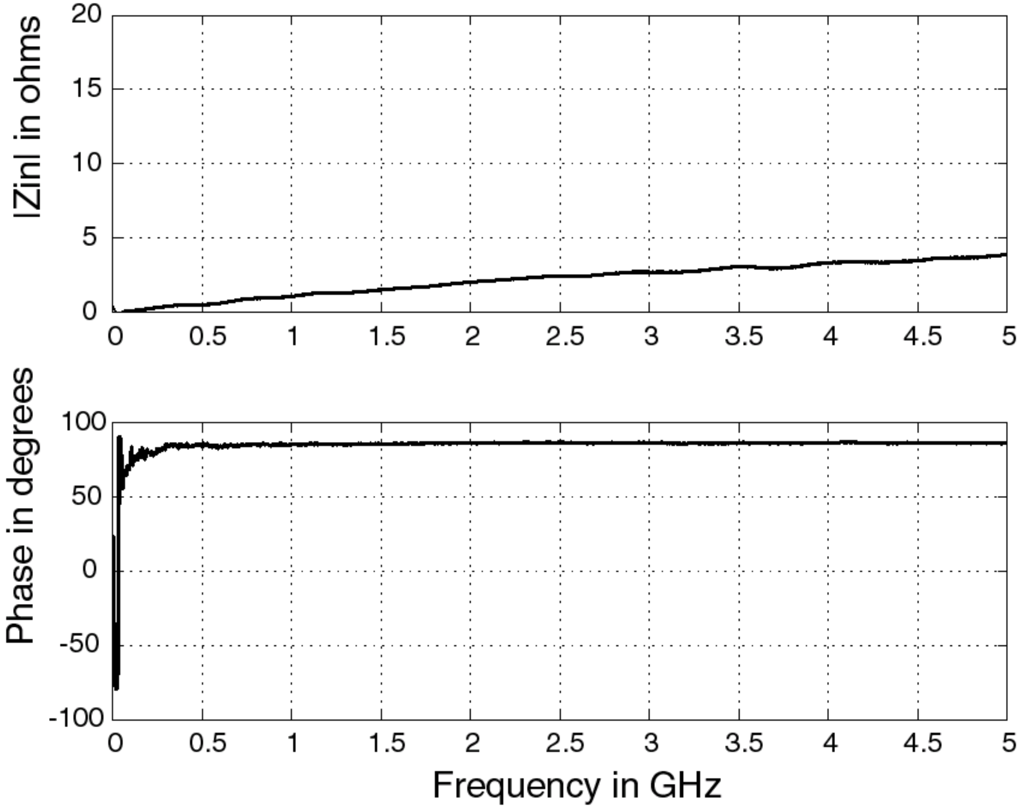
Power Bus Resonances

Input impedance of a populated 8” x 9” FR4 board with closely spaced (4.5 mil) planes



Power Bus Resonances

Input impedance of a populated 2” x 3” board with embedded capacitance



Do you need Power Planes?

Advantages of power planes	Disadvantages of power planes
Provides high-frequency current	Lower power bus impedance may increase current rise in devices, leading to stronger RF and EMI
Lower power bus impedance reduces noise voltage on power bus	Possibly higher layer count.
Easier to route power	Power bus resonances may radiate directly from the plane pair.
Large current handling ability	

Do you ever want a higher power bus impedance?

If planes are used, but components are not connected directly, then a connecting impedance (e.g., a small resistor or a ferrite bead) can be used to decouple the IC from the plane, or, to decouple the plane from the IC.

A local decoupling capacitor can be placed on the device side of the connecting impedance

BUT …

Do you ever want a higher power bus impedance?

DON'T CUT OR "MOAT" THE <u>GROUND</u> PLANE !

Power Bus Decoupling Strategy

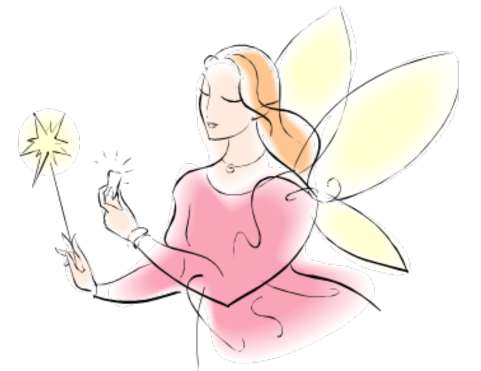
Low-impedance planes or traces?

- choice based on bandwidth and board complexity
- planes are not always the best choice

Planes widely spaced or closely spaced?

- want local or global decoupling?
- want stripline traces?
- lower impedances obtainable with closely spaced planes.

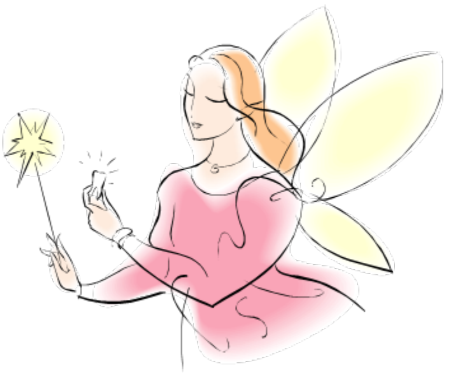
Decoupling Myths



In order to be effective, capacitors must be located within a radius of the active device equal to the distance a wave can travel in the transition time of the circuitry.

On boards with closely spaced planes (where this rule is normally applied) none of the capacitors on the board can typically respond within the transition time of the circuitry no matter where they are located.

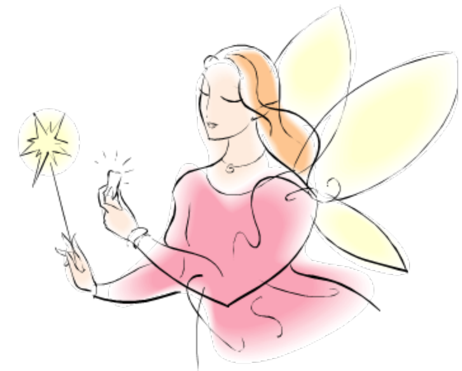
Decoupling Myths



Smaller valued capacitors (i.e. 10 pF) respond faster than higher valued capacitors.

The ability of a capacitor to supply current quickly is determined by its mounted inductance. The value of the capacitance only affects its ability to respond over longer periods of time. For a given value of inductance, higher valued capacitors are more effective for decoupling.

Decoupling Myths



Active devices should be connected with traces to the capacitor, then through vias to the power planes.

This sounds like a good idea until you apply some realistic numbers and evaluate the tradeoffs. In general, any approach that adds more inductance (without adding more loss) is a bad idea. Power and ground pins of an active device should generally be connected directly to the power planes.

Final Words

- Correct strategy **depends on plane spacing**!

- PCB Decoupling is mostly about capacitance at kHz frequencies
- PCB Decoupling is mostly about inductance at MHz frequencies
- PCB Decoupling is mostly non-existent at GHz frequencies