PDN Application of Ferrite Beads

11-TA3

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Objectives

- Understand ferrite beads with a good model
- Understand PDN design w/ sensitive loads
- Understand how to determine when a ferrite bead based filter makes sense and when it does not
- Understand filter synthesis to design req'ts
 - Summarized, details in manuscript

Ferrite Bead Properties

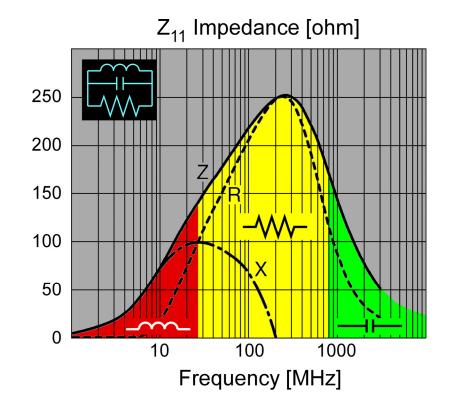
- Ferrite beads are not magic.
 - They are neither panaceas, nor or they demons from PDN hell.
- Ferrite beads are components like any others which have very useful properties, but impose side-effects which must be considered.
- Proper applications occur where the benefits outweigh the costs of the side-effects.

Ferrite Bead Properties

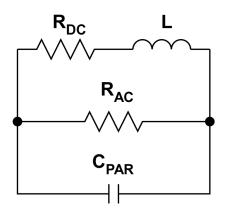
- Sintered compositions
- Two families dominate beads:
 - MnZn
 - Lower frequency power material
 - Lower resistivity
 - Higher permeability
 - NiZn
 - Higher frequency material
 - Higher resistivity
 - Lower permeability

Ferrites Make Excellent Inductors

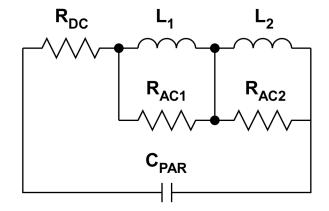
- Beads are typically resistive over 1-2 frequency decades
 - At lower frequencies they are inductive
 - At higher frequencies they are capacitive
- Some NiZn ferrite beads are high Q inductors well past 100MHz.
 - TDK MPZxxxxDyyy beads are inductive to 300-400MHz



Models

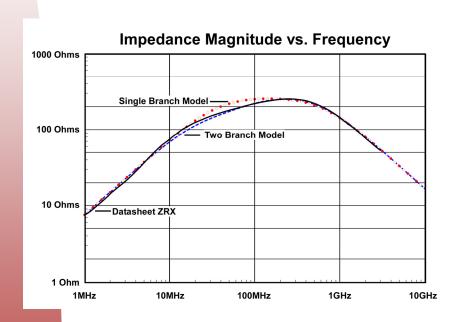


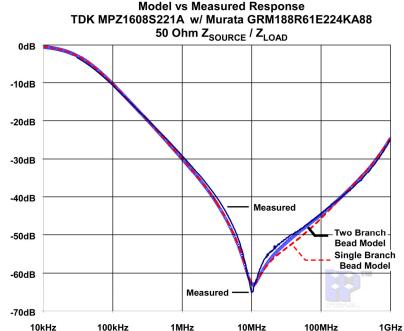
Single-Branch Model



Two-Branch Model

Example Model Fit



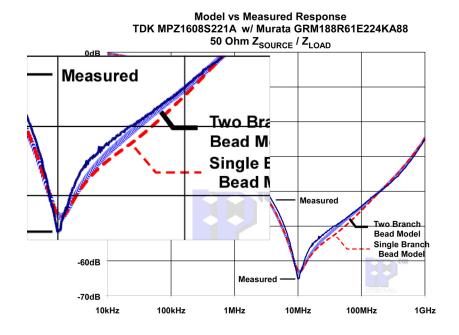


Component Only

Filter Response 50 Ohm Ports

Example Model Fit

 1 Branch and 2 branch models both closely track actual response with only minor variations deep in the stop band.



Filter Response 50 Ohm Ports

Available Bead Characteristics

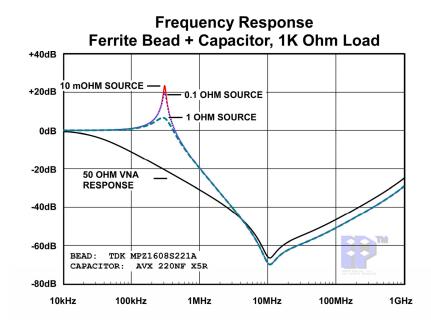
- Beads are available with equivalent inductances from 10's of nH to several uH.
- If lower inductance is needed, consider making an inductor out of a small etch segment:
 - $-L \approx \mu 0 * \mu r * H * L/W$
 - H Dielectric height in mils
 - L/W dimensionless length / width

DC BIAS

- Beads are subject to saturation effects
- DC bias above 30-40% of rated current can substantially drop effective inductance by 50% or more.
 - How much depends on how aggressively I_{MAX} has been rated.
 - Simulate with both min and max load currents
 - F_{co} shifts-up at higher biases
 - Q reduces at higher biases
 - Reduces insertion loss
- Beware of some vendor SPICE models for AC analysis
 - Some models have been developed for transient response and have questionable AC response.
 - Best to derive performance from measurements or data sheet ZXR or S params at required bias.

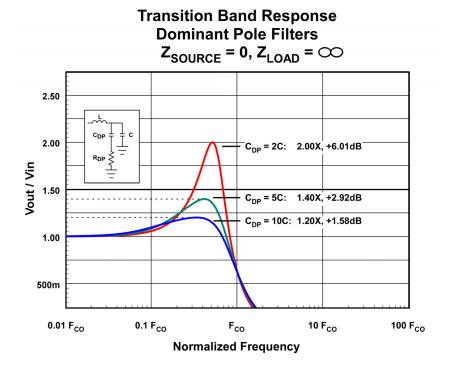
LPF F_{CO} Resonance

- Lightly loaded series LC filters resonate
- Ferrite beads high Q inductor at F_{co} for most applications
- Lots of noise insertion gain is possible near F_{co}
- For PLLs this can be very problematic, especially when F_{co} is located close to a noise source like an SMPS switching frequency.



Damp LC Filters w/Dominant Poles

- Dominant pole advantages:
 - No added DC drop
 - No insertion loss reduction in stop-band
 - No added DC power consumption
- Disadvantages
 - Additional larger capacitor required to form the dominant pole
- C_{DP} = 5C is usually a good design compromise
 - $-C_{DP}$, R_{DP} tables in manuscript

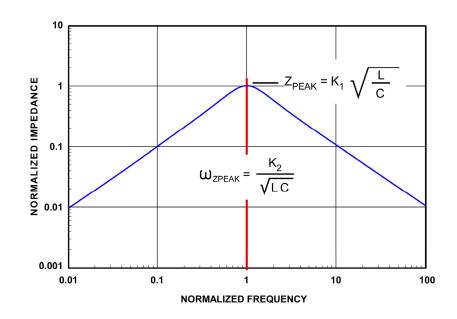


Series Filter Z₂₂ Impedance

- Series filter load side shunt impedance builds to a maximum near F_{CO}.
- More inductance =>
 - Lower FCO,
 - More outside noise insertion loss,

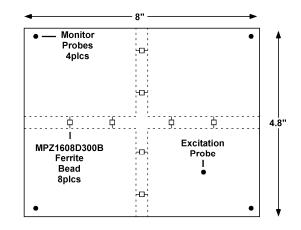
BUT ALSO

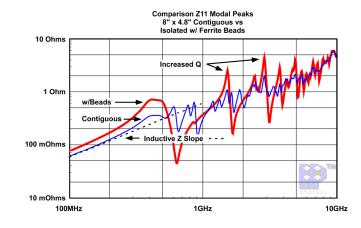
- Higher load side impedance
 - Load side capacitance must scale w/series inductance to hold a fixed maximum Z₂₂



Local Plane Isolation w/ Beads

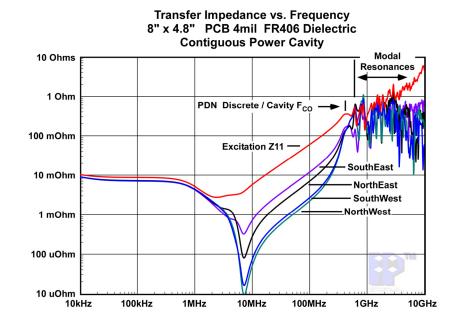
- Contiguous planes versus four quadrants
 - Total is greater than sum of the parts
- Larger plane extents suppress modal resonances:
 - Skin and tangent loss both increase each reflection pass for larger dimensions
 - Smaller polygons:
 - Less loss / pass
 - Higher Q
 - More resonant peaking





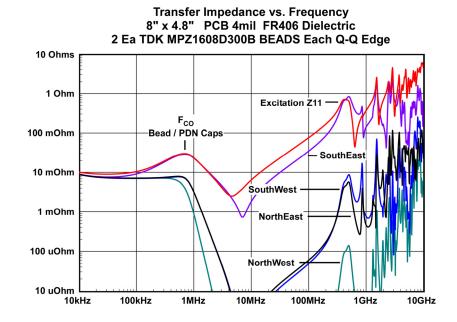
Local Plane Isolation w/ Beads

- Example uniform bypass:
 - 2 ea 1uF 0402 / sq in.
 - 500uF 7mOhm each quadrant
- w/o beads, excited source sees the entire PDN
 - Lower effective Z up to PDN / PCB resonance
 - Little isolation at PDN/PCB resonance and lower modal resonance frequencies



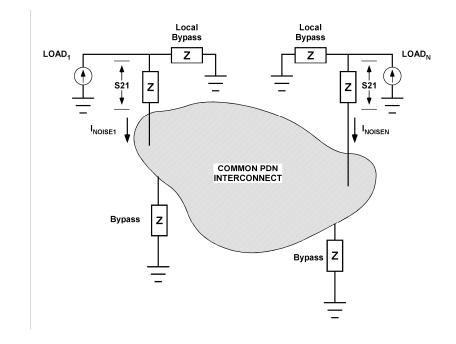
Local Plane Isolation w/ Beads

- w/ beads, excited source sees the entire PDN only up to about ½ F_{co}.
 - Higher impedance at all higher frequencies than w/o bead.
 - Other quadrants isolate@ FCO and beyond
 - High isolation through
 PDN resonance, and PCB modal resonances.



When **Doesn't** Series Isolation Make Sense?

- Loads that tolerate similar noise levels at the common PDN interconnect (planes) do not benefit from isolation.
 - Z_{BYPASS} for each load is inversely proportional to that load's noise current.
 - F.O. approximation bypass is the same joined or isolated.
 - Actually better joined:
 - Noise coherence or lack thereof



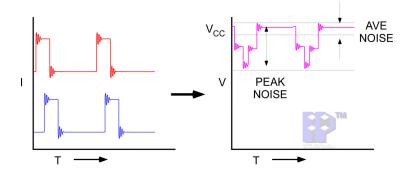
Combined Noise Sources, Equal Noise Tolerance @PCB

- Loads that tolerate similar noise levels at the common PDN interconnect (planes) require bypass admittance proportional to noise current.
- IE constant peak noise voltage.

COMBINED NOISE SOURCES & BYPASS
RESISTIVE PDN
COHERENT, PHASE-ALIGNED NOISE SOURCES

VCC
V PEAK
NOISE
T T T

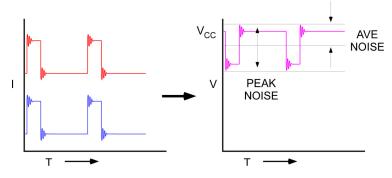
COHERENT, PHASE-UNALIGNED NOISE SOURCES



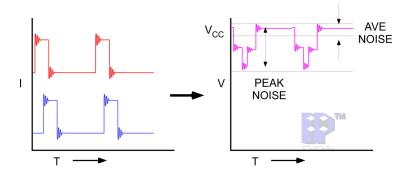
Combined Noise Sources, Equal Noise Tolerance @PCB

- When connected together, the *PEAK* noise remains constant
- Average voltage ONLY remains constant if the noise sources are coherent and in-phase.
- Out of phase reduces average noise.
- Incoherent drives average noise down by square root of equal sources w/ matched bypass

COMBINED NOISE SOURCES & BYPASS RESISTIVE PDN COHERENT, PHASE-ALIGNED NOISE SOURCES



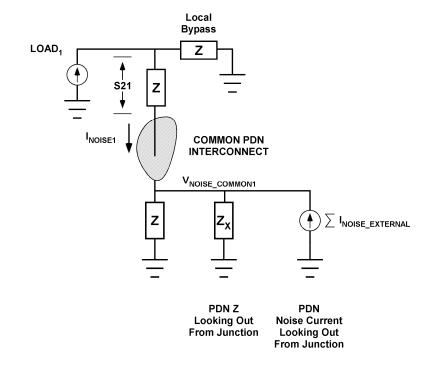
COHERENT, PHASE-UNALIGNED NOISE SOURCES





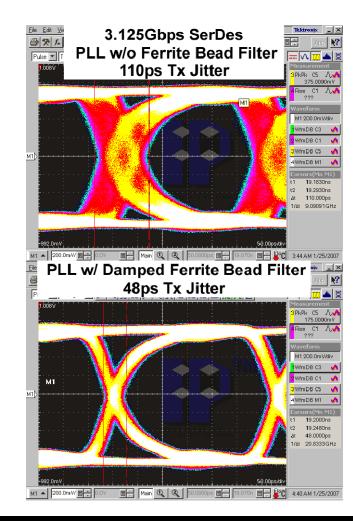
When **Does** Series Isolation Make Sense?

- Loads that do not tolerate similar noise levels at the common PDN interconnect (planes), and where the more sensitive load current does not heavily dominate.
- More tolerant loads are overbypassed to meet sensitive load noise requirements.
- Isolation can result in component reductions of 5:1 or more.



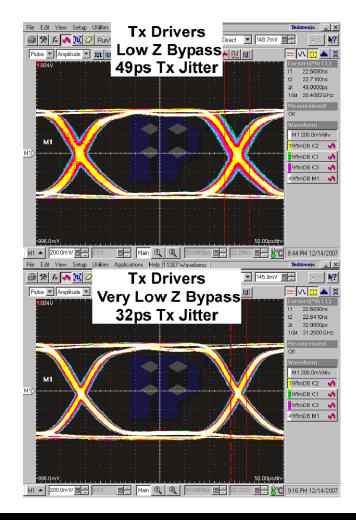
Example PLL Noise Sensitivity

- PLL supply well bypassed in both cases.
- Top:
 - PLL supply common w/digital supply
- Bottom:
 - PLL supply isolated w/ damped ferrite bead filter
- Ferrite bead based series filter is well-justified in this application.



Example Z₂₂ Impedance Sensitivity

- Different SerDes than previous example.
- Transmit jitter source is primarily ISI.
- Top:
 - Low impedance PCB AVCCH supply
- Bottom:
 - Improved very low impedance
 PCB AVCCH supply
- Ferrite beads would aggravate ISI by raising Z₂₂
- Don't starve high-speed circuits!



PDN Example, Bead Evaluation

- Analog load: High speed ADC
 - $-+/-2mV V_{CC}$ noise tolerance
 - +/-100mA dynamic current
 - 20mOhms Z_{MAX}
- N 1.2V Digital I/Os:
 - -+/-30mV V_{cc} noise tolerance
 - +/-N*10mA dynamic current
 - $@ +/-2mV Z_{MAX} = 0.2 Ohms/N$
 - $@ +/-30 \text{mV Z}_{MAX} = 3.0 \text{ Ohms/N}$

Example

- FOM
 - # of bypass caps required = K/FOM
- Common rail
 - 10 I/Os 20mOhms digital, 20mOhms analog
 - $FOM = (.02 \mid | .02) = .010$
 - 100 I/Os 2mOhms digital
 - $FOM = (.02 \mid | .002) = .0018$
- Isolated rails
 - 10 I/Os 20mOhms analog, 300mOhms digital
 - $FOM = (.02 \mid | 0.30) = .019$
 - $.019/0.010 \approx 1.9:1$ component reduction by isolation
 - 100 I/Os 20mOhms analog, 30mOhms digital
 - $FOM = (.02 \mid | .03) = .012$
 - $.012/0.0018 \approx$ **6.7:1** component reduction by isolation

Filter Synthesis Summary

- Full synthesis procedure detailed in manuscript
- Step #1:
 - Determine the design requirements:
 - How much noise does the analog node tolerate vs frequency at the PCB attachment?
 - Translate to insertion loss
 - What is the current vs. frequency from the analog node?
- Without requirements:
 - Do Not Pass Go, Do Not Collect \$200.

Filter Synthesis Summary

- Choose the lowest inductance bead that will do the job
- Load side capacitance determined by the greater req't:
 - Bead inductance and Z₂₂ low frequency impedance requirements
 - Bead inductance and F_{co} requirements.
- Dominant pole damping req'd/not req'd determined by bead L / bypass C Q near F_{co}
 - See manuscript for details
- Load side HF capacitor count determined by Z₂₂ vs. high frequency requirements.



Summary

- Ferrite beads are not magic.
- Ferrite beads can be modeled relatively simply for modest DC current swings.
 - Multiple sim passes required if the load has wide DC swing
- Ferrite beads are high Q inductors up to some frequency that depends on the bead material.
 - Some beads are high Q inductors to 100's of MHz
 - More typical is 10MHz 30MHz
 - Series filter design must account for damping req'ts at F_{co}.
 - Dominant pole is usually the best damping technique when req'd.



Summary Cont'd

- Make PDN no more complex than actually needed.
 - Series filters / partitioning can realize very high noise isolation from low to high frequencies.
 - Series filters and rail partitioning aggravate:
 - Signal return routing
 - Layout
 - Noise averaging
 - PCB modal resonances
 - Larger polygons / planes serving more properly bypassed loads yield the lowest average noise levels for a given PDN bypass component count.

Summary Cont'd

- The need for a series filter can only be determined when power delivery requirements are known.
- Series filters make sense only when:
 - Noise voltage sensitivity at the planes is disparate AND
 - The less sensitive loads dominate noise currents
- Always design series filters for the minimum required insertion loss / inductance to do the job.
 - Sometimes a small etch inductor will do better than a bead due to available small inductances.
- KNOW YOUR POWER DELIVERY REQUIREMENTS!



Thank You

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