UNIVERSITY OF TWENTE, ENSCHEDE

TELECOMMUNICATION ENGINEERING GROUP

FACULTY OF EEMCS

Printed Circuit Boards

for the Education aimed at

Understanding Electromagnetic Effects

User Manual

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Introduction

Demos are often used in electromagnetic (field) courses. We have developed many types of demos and used also demos developed by others, such as those described in the IEEE EMC Education Manual [IEEE04] and [IEEE92], or the demo developed within the ASIAN-EU University Network Program [ASEU], or within PATON [PATON09]. Two main drawbacks could be observed:

1. We could easily show the fundamental aspects such as Lenz Law, or crosstalk, in an idealized world, but this was not taken for granted by practicing engineers: these engineers needed a link to their own world. Especially people involved in signal and power integrity issues, ground bounce and interconnects: Their world is often a printed circuit board.

2. The size of many of the demos is huge. Transportation of such demos is therefore a problem.

Hence we decided to develop a series of demos on Eurocard (100x160mm) printed circuit boards (PCB) [KNIJF05]. Test equipment consists in most cases of a basic generator, a dual channel oscilloscope, and, if available, a basic spectrum analyzer. The demo kit has been presented at several EMC conferences [LEFea08], [LEF09] [BUE809] and [BUE909] and many, many people were interested. Therefore a new generation was developed. The detailed description of these new demo PCBs is presented in this document in Chapters 1 through 9. Table 1 shows where the descriptions can be found in this manual.

Table 1: Survey of Currently Available EMC Demo Boards

Over time new experiments will emerge. The Ground Bounce experiments, as an example, now exist in two versions. The second version is labelled Mk2 (Mark 2) to distinguish it from its predecessor.

Acknowledgements

We wish to thank all who contributed to the realization of the EMC Demonstration PCB set.
In particular:

- Prof. Dr. Frank Leferink MSc.
- Istwaan Knijff MSc., Martijn Brethouwer
- Christiaan Teerling, Eduard Bos
- Frank Wiggers, Gerald Hoekstra

Contents

Chapter 1

Self Induction Board

Contents

1.1 Demonstrations on the Self Induction Board.

This demonstration board shows that all conductor loops have self induction. Cause is the magnetic field that inherently accompanies any current. It manifests itself when a step voltage change is applied to the input terminals of the loop. Initially, the loop generates a voltage proportional to the change in magnetic flux. This prevents the current from following the voltage step immediately. This is described by Faraday's Law. The duration of this transient voltage depends on the area of the loop. Induction can be used to delay (remove high frequencies in) current change.

1.2 Self Induction Board Views

1.2.1 The Finished Board

The end result of the assembly of the Self-Induction Board is shown in Figure 1.1.

Figure 1.1: The Finished Self-Induction Board.

1.2.2 The Silkscreen

The Silkscreen of the Self-Induction Board shown in Figure 1.2 points out which components should be mounted where:

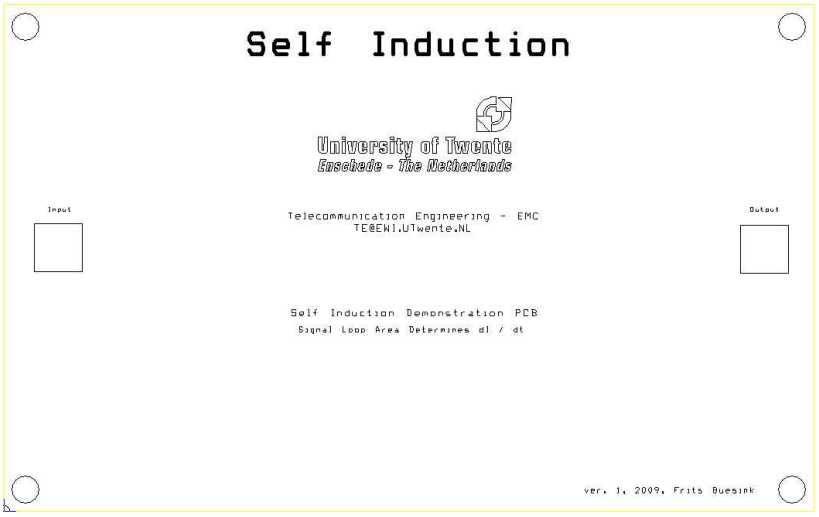

Figure 1.2: The Self-Induction Board Silk Screen.

1.2.3 Bare Board Top View

The etch pattern of the empty board, seen from the top side, is shown in Figure 1.3.

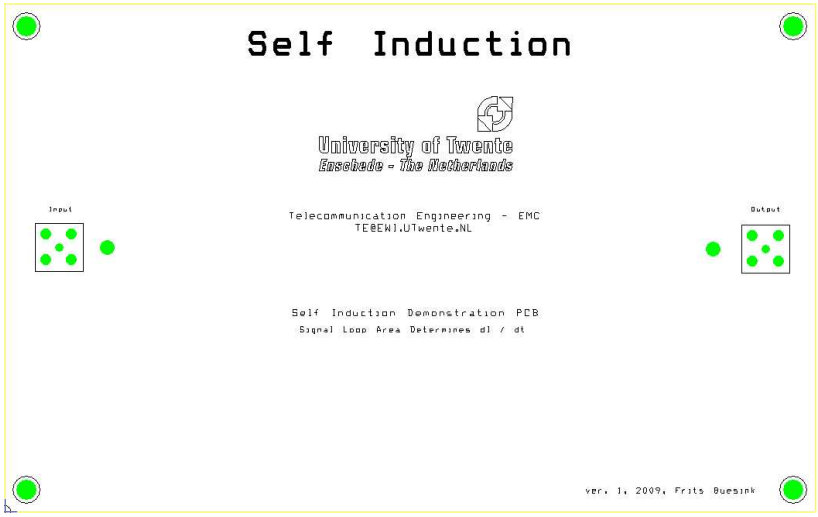

Figure 1.3: The Self-Induction Bare Board (Top View)

1.2.4 Bare Board Bottom View

The etch pattern of the empty board, seen from the bottom side, is shown in Figure 1.4.

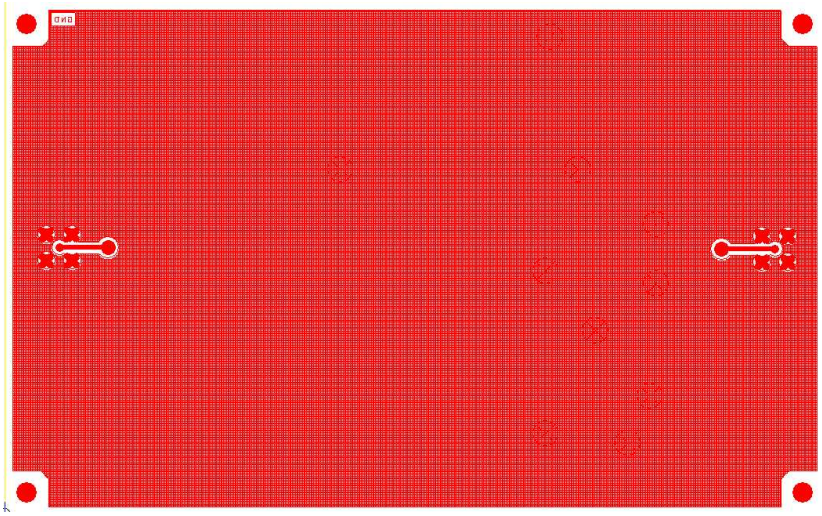

Figure 1.4: The Self-Induction Bare Board (Bottom View)

1.2.5 The Board Schematic

The schematic diagram of the Self-Induction board is essentially two connectors with a connecting wire, see Figure 1.5

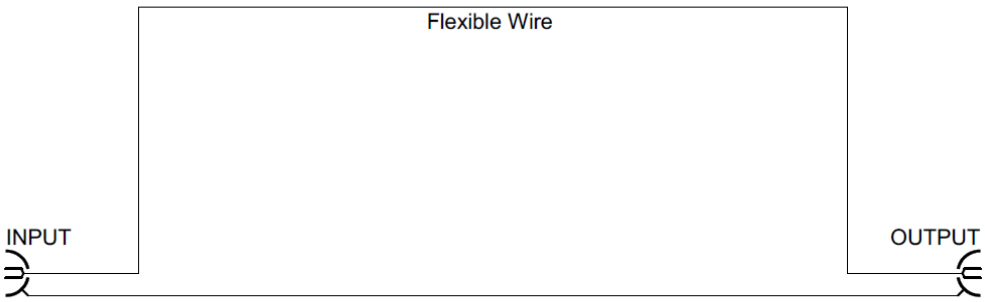

Figure 1.5: The Self-Induction Board Schematic.

1.2.6 The Bill of Materials

The bill of materials is shown below as Table 1.1

Table 1.1: Bill of Materials of the Self Induction Board

REF DES	VALUE
Input	SMB
Output	SMB
–	35 cm of flexible wire

1.3 Board Functional Description

The Self-Induction board demonstrates Faraday's Law and the Proximity Effect. It is a basic introduction to the Lenz's Law Board described in Chapter 2. Faraday's Law describes the phenomenon that a voltage is induced in a (wire-) loop due to a change in the magnetic flux that is enclosed by the loop. The Self Induction Board and the Lenz' Law Board both show this phenomenon in the opposite direction: if a voltage step is applied to the input terminals of an interconnection it takes some time before current starts to flow. For this demonstration the interconnection formed by a single signal wire plus return ground plane is loaded with 50Ω. A generator with, again, 50Ω is used to feed a voltage step (actually: a square wave) into the wire + ground loop. The 50Ω impedances imply a equilibrium signal voltage of 50% of the unloaded source amplitude. The loop self inductance provides a reverse voltage, initially equal to the source voltage. As the current (and magnetic field) in the loop builds up, the voltage reduces (as a decaying exponential) toward the equilibrium

voltage determined by the source and load internal impedances. At the load side, initially no currents flows and the voltage over the load resistor hence starts out at zero. After that this voltage increases, as a mirror image of the voltage at the source end, towards the equilibrium voltage. The physical loop is formed by a flexible wire over a ground plane (see Figure 1.1). A square wave generator with 50Ω internal impedance is connected via channel 1 of a dual channel oscilloscope to the input connector using a T-junction. This channel 1 must be high-impedance in relation to the characteristic impedance of the connecting 50Ω cable. The output is connected to channel 2 of the oscilloscope with another 50Ω cable. This channel 2 must be switched to 50Ω or be provided with a 50Ω feed-through load. This is shown in Figure 1.6. An oscilloscope with a bandwidth of 200 MHz or more is required while the generator must have a rise-time of around 10 ns or less. The setup of the oscilloscope and generator for measurements in the time domain, described here, corresponds to the arrangement of a Time Domain Reflectometer (TDR). Such an instrument could be used to perform this same experiment. The oscilloscope is adjusted to a time-base of 100 ns/DIV and the amplitude of the channels appropriate for the output level of the generator. The oscilloscope picture in Figure 1.8 shows the resulting waveforms for a large loop area. After the wire is placed against the ground plane over its full length (!), the picture changes to that in Figure 1.9. Note: The trace on the top is the "1" channel (input) while the trace on the bottom is the output on channel "2".

Another experiment option is to analyze the board in the frequency domain. For that purpose a spectrum analyzer with tracking generator is used. Three wire arrangements have been measured:

1. A wide loop, the wire is far removed from the ground plane
2. A minimal loop, the wire is meandering on the surface of the board, close to the ground plane
3. A random loop, the wire is left as it rests on the board, sometimes touching, at other places floating in space

The spectrum analyzer is calibrated to show a horizontal 0 dB line if the tracking generator is connected directly to the input. The results for the three situations are shown in Figure 1.10. For the

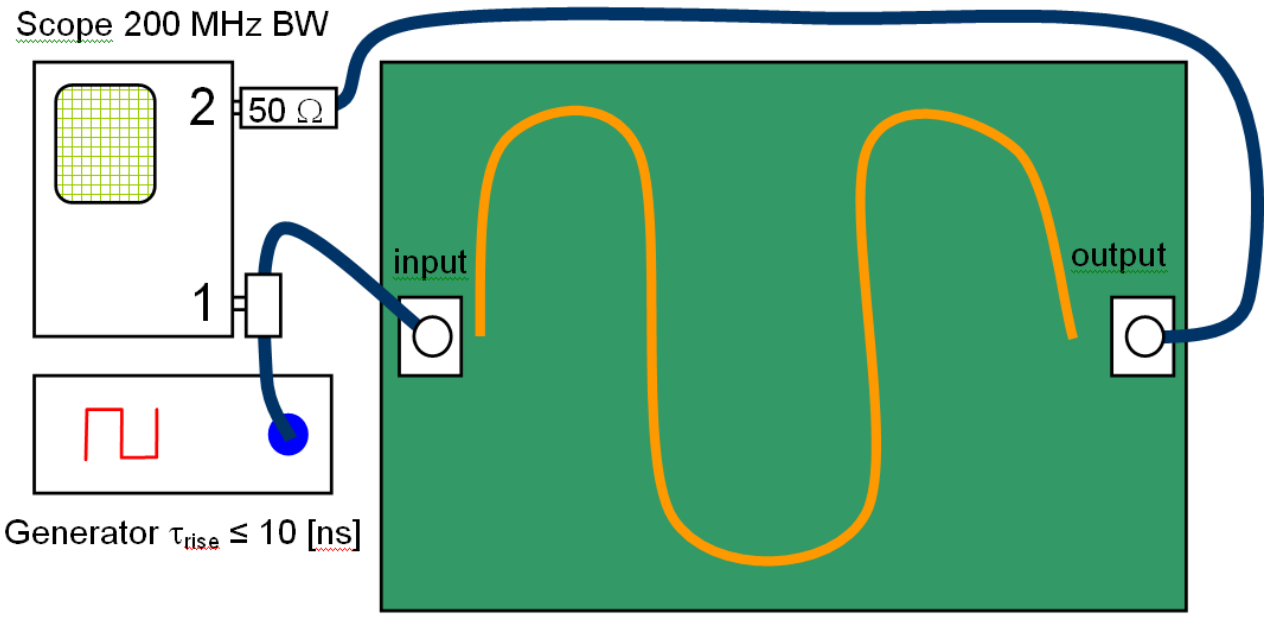

Figure 1.6: Connection Diagram for Self-Induction Experiment.

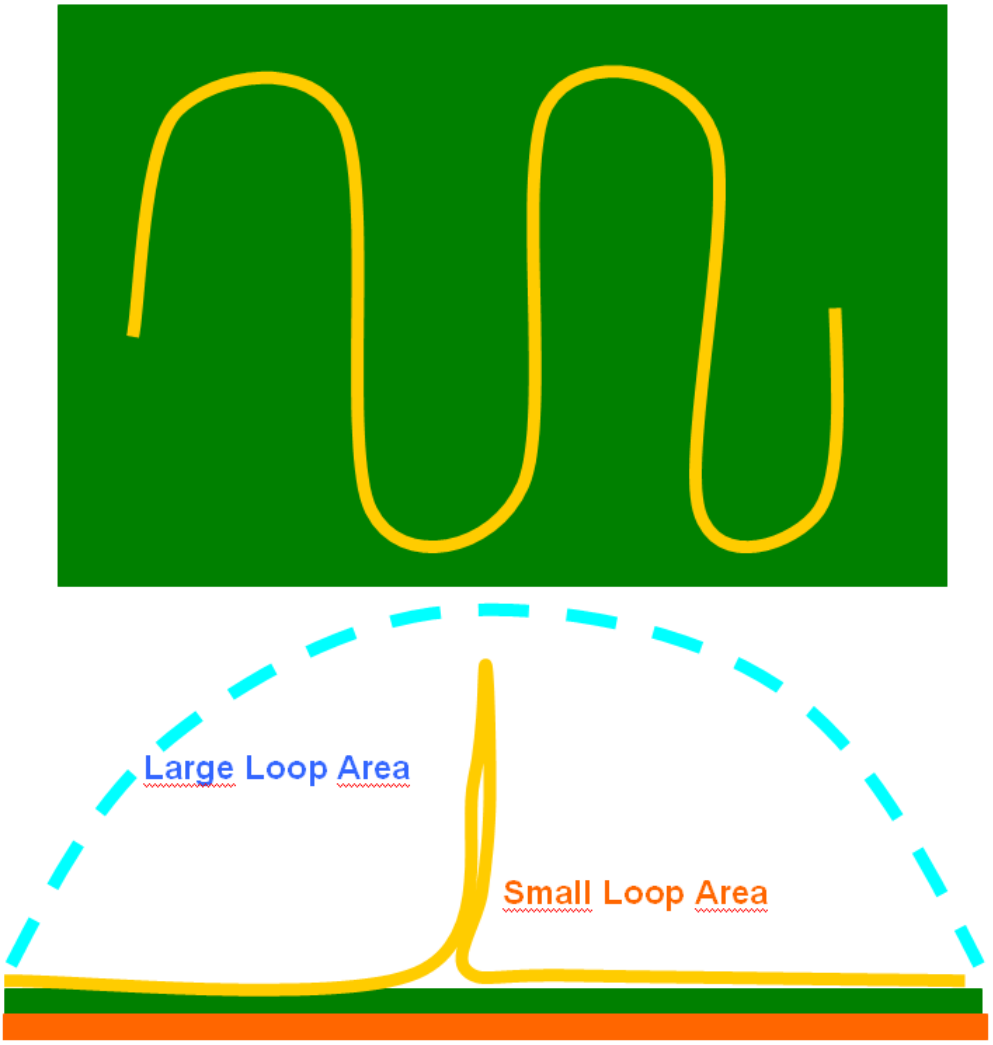

Figure 1.7: Two possible ways to reduce loop area.

interpretation of the graph it is important to remember that the wire + ground-plane combination is actually intended as an interconnection, a transmission line. The ideal transmission line passes all frequencies with 0 dB attenuation. For comparison, this ideal “0 dB” line has been added to the graph in Figure 1.10. It is obvious from the measurements that the position of the wire with the smallest loop area approaches this ideal line best. The largest wire loop has the worst performance (maximum attenuation). The randomly positioned wire ends up somewhere between the best and the worst case.

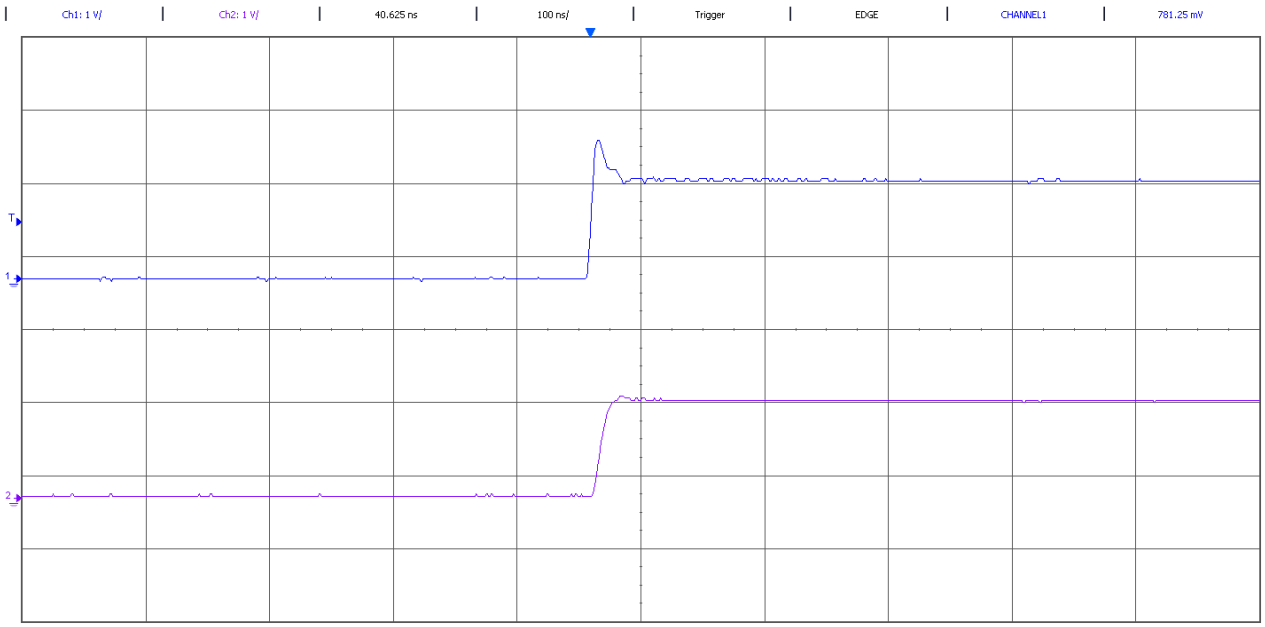

Figure 1.8: Oscilloscope picture for a large loop area.

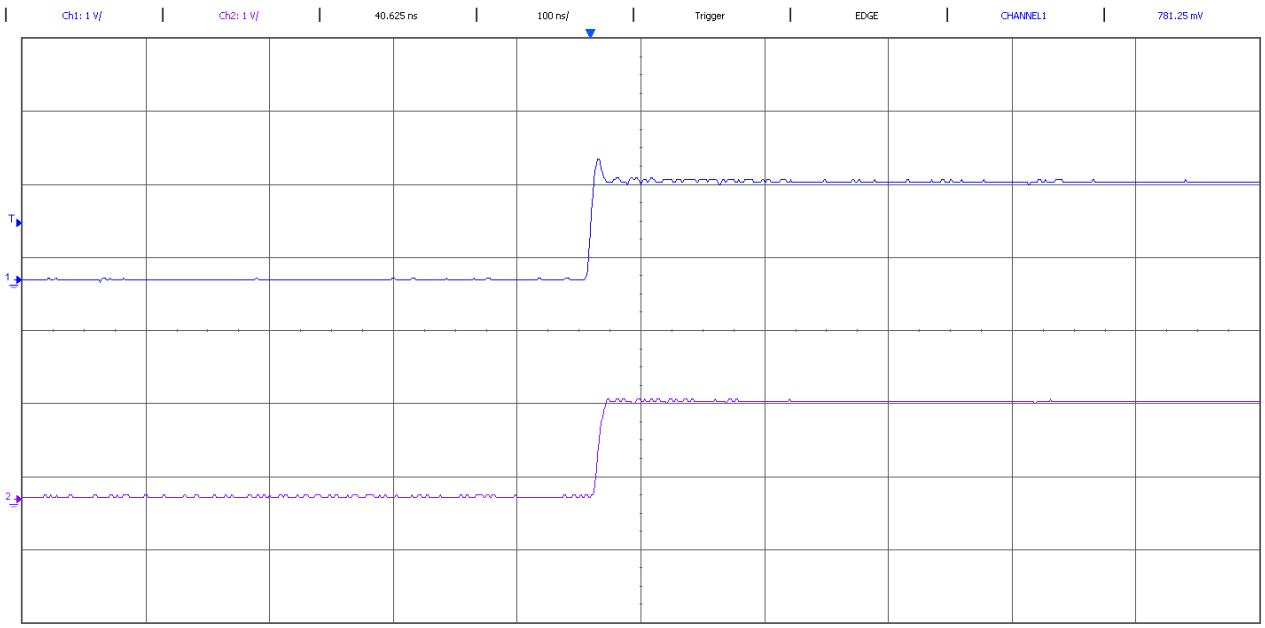

Figure 1.9: Oscilloscope picture for a small loop area.

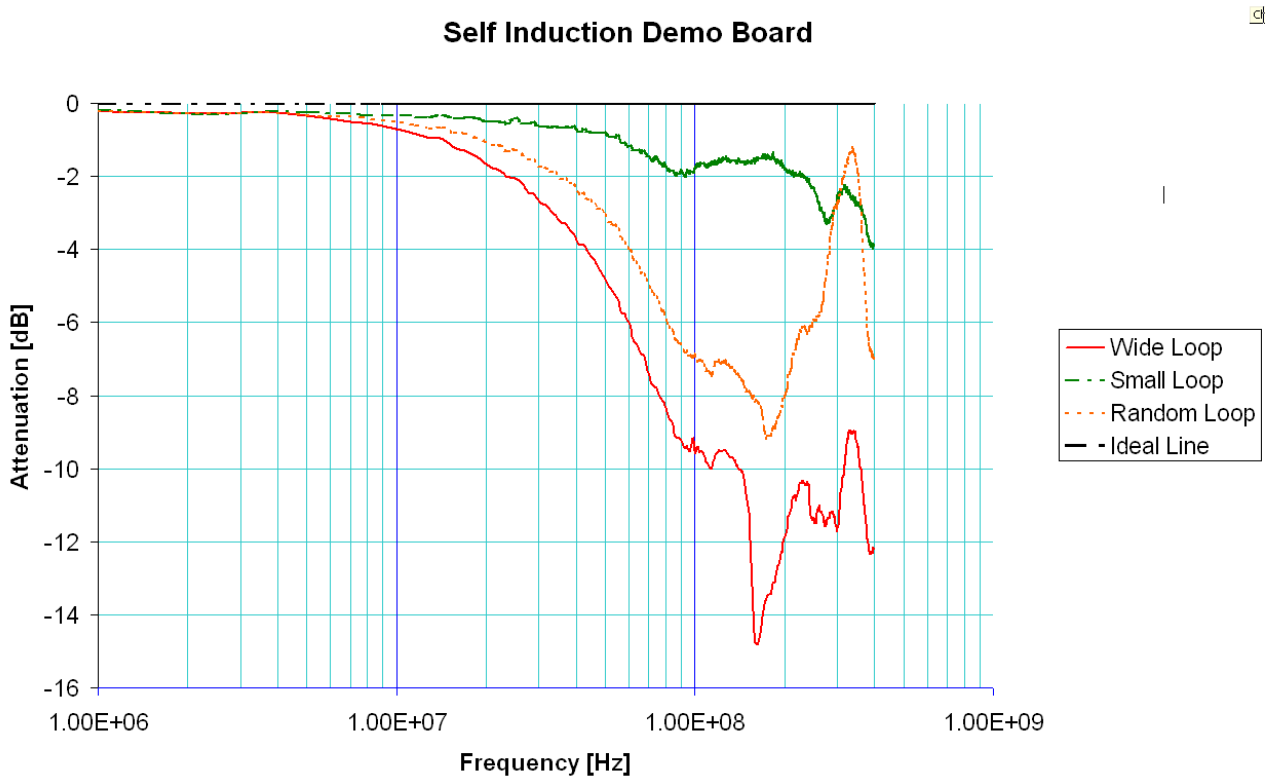

Figure 1.10: Attenuation as function of frequency for various wire locations.

1.4 Lessons Learned

Using the Self-Induction experiment we have learned that:

1. The Self Induction of a loop formed by the signal and return conductor of an interconnection can disturb the signal integrity by attenuating the higher frequencies.
2. This is caused by the energy stored in the magnetic field associated with the signal current over the interconnection. The buildup and dissolution of this field takes time.
3. The magnetic field generated by the interconnection can affect other systems in the environment.

Chapter 2

Lenz' Law

Contents

2.1 Demonstrations on the Lenz' Law Board

The Lenz'Law Board demonstrates the same phenomena as the Self Induction Board. Instead of a flexible wire (-loop) a number of traces are laid out on the board to show essentially the same aspects: currents prefer the path of least inductance. If the inductance is high, it will take more time to reach the steady state current level after a voltage step at the source connection. For a trace over a wide ground plane (=transmission line) the transition is almost instantaneous.

2.2 Lenz'Law Board Views

2.2.1 The Finished Board

The end result of the assembly of the Lenz' Law Board is shown in Figure 2.1.

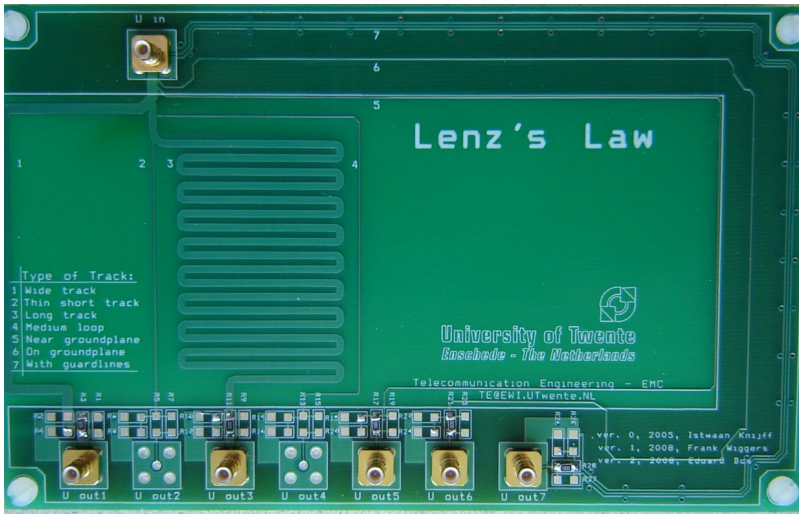

Figure 2.1: The Finished Lenz' Law Board.

2.2.2 The Silkscreen

The Silkscreen of the Lenz' Law Board shown in Figure 2.2 points out which components should be mounted where:

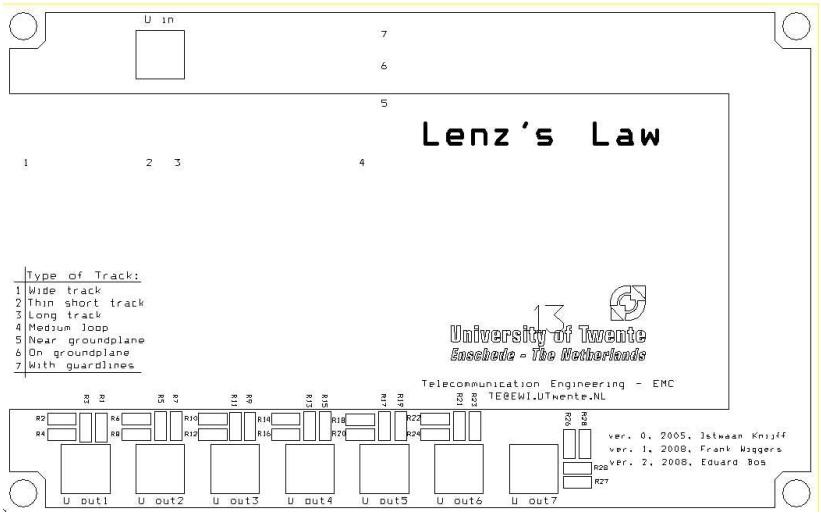

Figure 2.2: The Lenz'Law Board Silk Screen.

2.2.3 Bare Board Top View

The etch pattern of the empty board, seen from the top side, is shown in Figure 2.3.

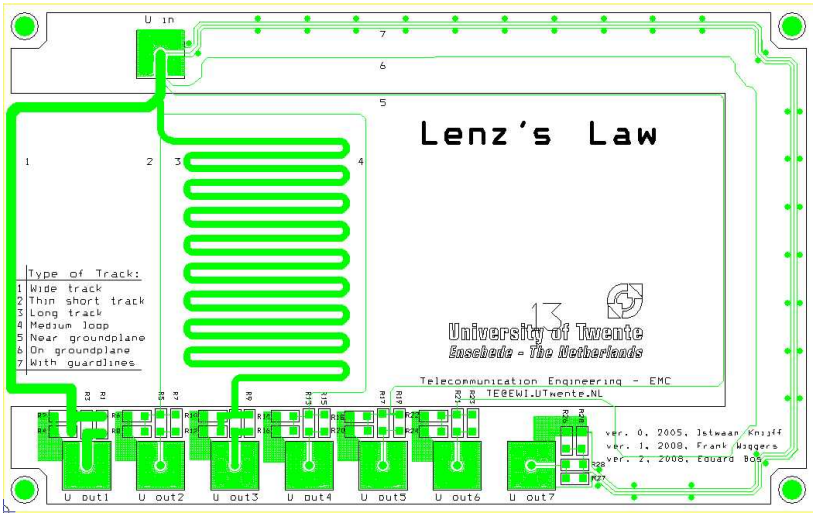

Figure 2.3: The Lenz's Law Bare Board (Top View)

2.2.4 Bare Board Bottom View

The etch pattern of the empty board, seen from the bottom side, is shown in Figure 2.4.

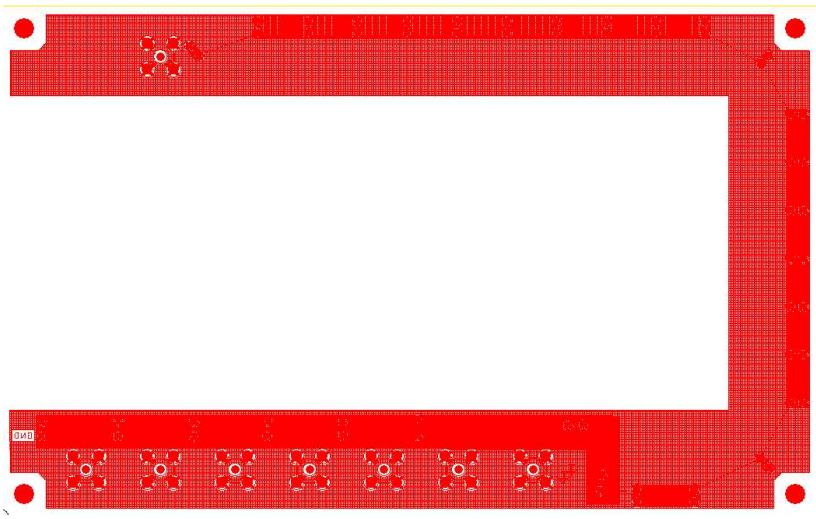

Figure 2.4: The Lenz's Law Bare Board (Bottom View)

2.2.5 The Board Schematic

The schematic diagram of the Lenz' Law board is shown in Figure 2.5. It is drawn in the way the board will be used in the functional description in section 2.3.

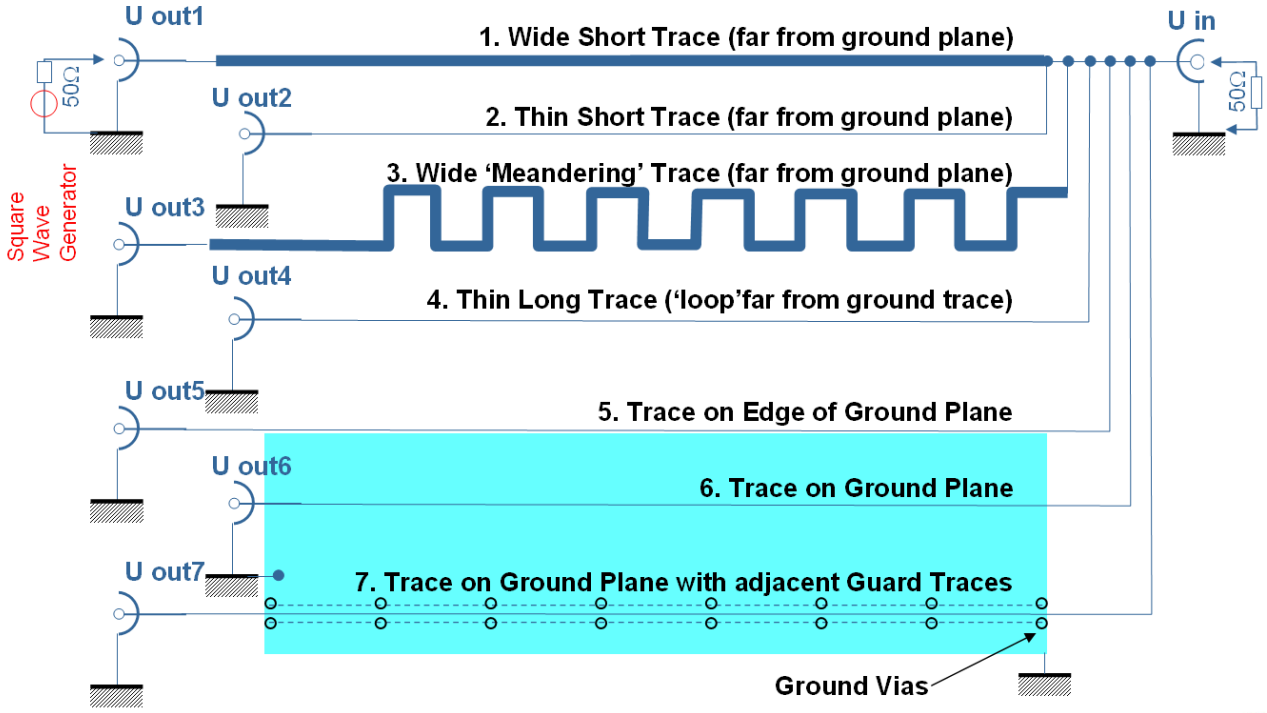

Figure 2.5: The Lenz' Law Board Schematic.

2.2.6 The Bill of Materials

The bill of materials of the Lenz's Law Board is shown below as Table 2.1.

Table 2.1: Bill of Materials of the Lenz's Law Board

REF DES	VALUE	PACKAGE	FOOTPRINT
U in	SMB	SMB	RF/SMB/V
U out1	SMB	SMB	RF/SMB/V
U out2	SMB	SMB	RF/SMB/V
U out3	SMB	SMB	RF/SMB/V
U out4	SMB	SMB	RF/SMB/V
U out5	SMB	SMB	RF/SMB/V
U out6	SMB	SMB	RF/SMB/V
U out7	SMB	SMB	RF/SMB/V
R1	0Ω	R	SM/R_1206
R2	not used	R	SM/R_1206
R3	not used	R	SM/R_1206

Table 2.1: Bill of Materials of the Lenz's Law Board (cont'd)

REF DES	VALUE	PACKAGE	FOOTPRINT
R4	not used	R	SM/R_1206
R5	not used	R	SM/R_1206
R6	not used	R	SM/R_1206
R7	0Ω	R	SM/R_1206
R8	not used	R	SM/R_1206
R9	0Ω	R	SM/R_1206
R10	not used	R	SM/R_1206
R11	not used	R	SM/R_1206
R12	not used	R	SM/R_1206
R13	not used	R	SM/R_1206
R14	not used	R	SM/R_1206
R15	0Ω	R	SM/R_1206
R16	not used	R	SM/R_1206
R17	not used	R	SM/R_1206
R18	not used	R	SM/R_1206
R19	0Ω	R	SM/R_1206
R20	0Ω	R	SM/R_1206
R21	not used	R	SM/R_1206
R22	not used	R	SM/R_1206
R23	not used	R	SM/R_1206
R24	not used	R	SM/R_1206
R25	not used	R	SM/R_1206
R26	not used	R	SM/R_1206
R27	not used	R	SM/R_1206
R28	0Ω	R	SM/R_1206

Of the 28 resistor positions on the board only seven are used. These are zero Ohm jumpers to connect the individual traces to the respective connectors.

2.3 Board Functional Description

The Lenz' Law board is (more or less) a "Frozen" version of the Self Induction Board. The various locations of the wire in the Self-Induction experiment are replaced by fixed etch patterns on the board. Some traces have a ground plane underneath, others do not. The bare board has one input connector (U in) and seven output connectors (U out1 through U out7). Each trace end has a voltage divider built up with four resistors feeding the output connectors as shown in Figure 2.6. These resistors can be used to fine tune the attenuation and impedance of each output. During our experiments it turned out that the basic function of the board can be demonstrated just as well and in line with the Self Induction experiment if the output connectors are used as inputs! This shows that the PCB demonstration boards are a living collection that is adapted to the needs of the day. The resistive voltage divider is hence not used here. It is replaced by a jumper (0Ω). In the

Bill of Materials (see section 2.2.6) these are indicated as R_1206 SMD resistors. These do exist. But a wire jumper will work just as well. The schematic diagram in section 2.2.5 does not show the resistive dividers. On the assembled board in Figure 2.1 not all U out connectors have been installed either. U out2 and U out4 were left out because the measured signals did not differ much from the neighboring traces. This could be different if a faster oscilloscope is used. The connectors should be mounted in the latter case. The measurement approach is the same as for the Self Induction Board. For the time-domain, the oscilloscope and generator are connected as shown in Figure 1.6 on page 5, with the remark that what is called "Input" in that figure, is now one of the U "outx" connectors. And of course, "Output" now becomes "U in". The step response results in the time domain for the 5 outputs 1, 3, 5, 6 and 7 are shown in Figures 2.7, 2.8, 2.9, 2.10 and 2.11

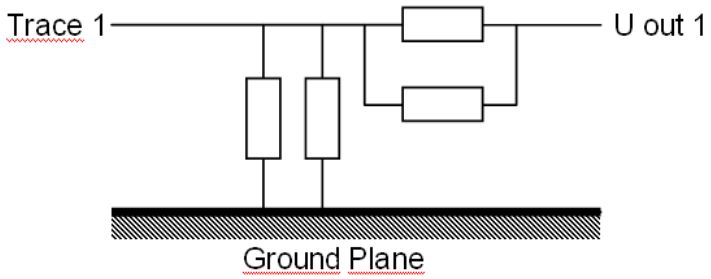

Figure 2.6: The (optional) resistive divider, one per output connector

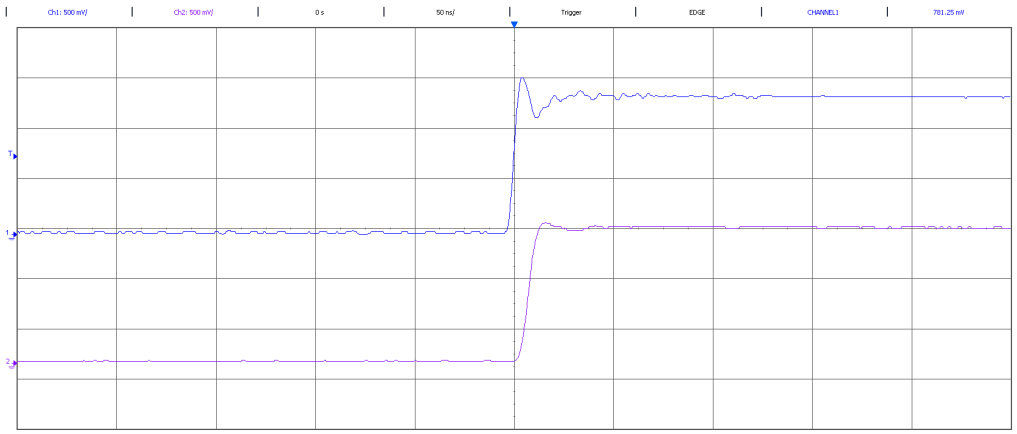

Figure 2.7: Step response of line 1

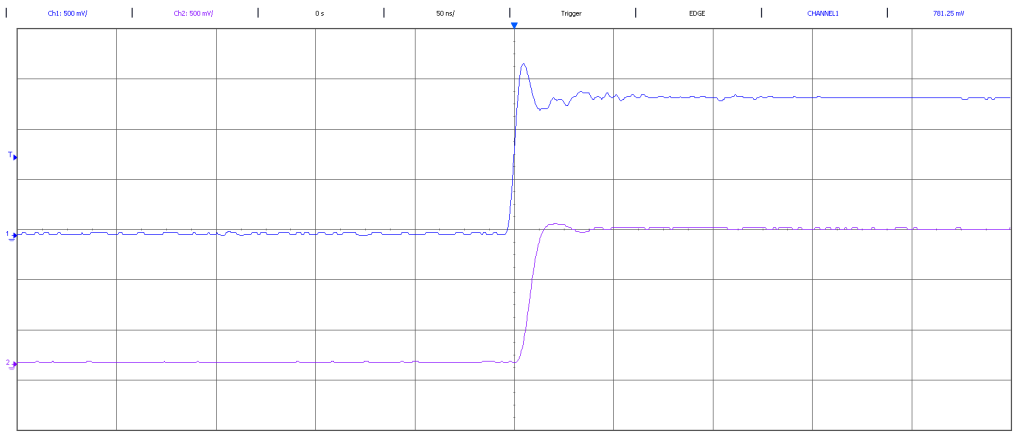

Figure 2.8: Step response of line 3

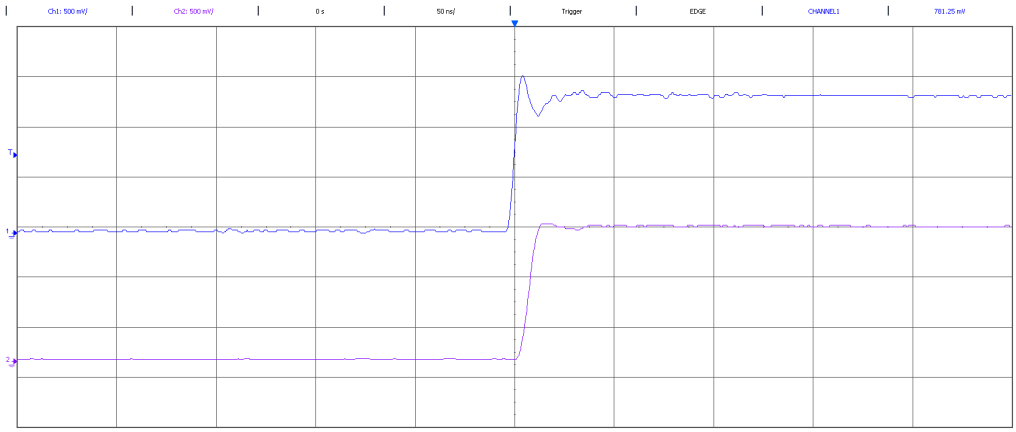

Figure 2.9: Step response of line 5

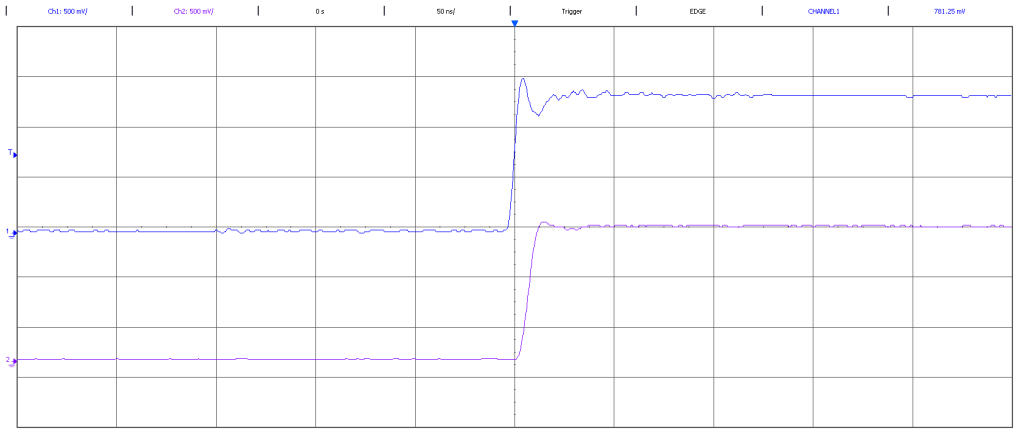

Figure 2.10: Step response of line 6

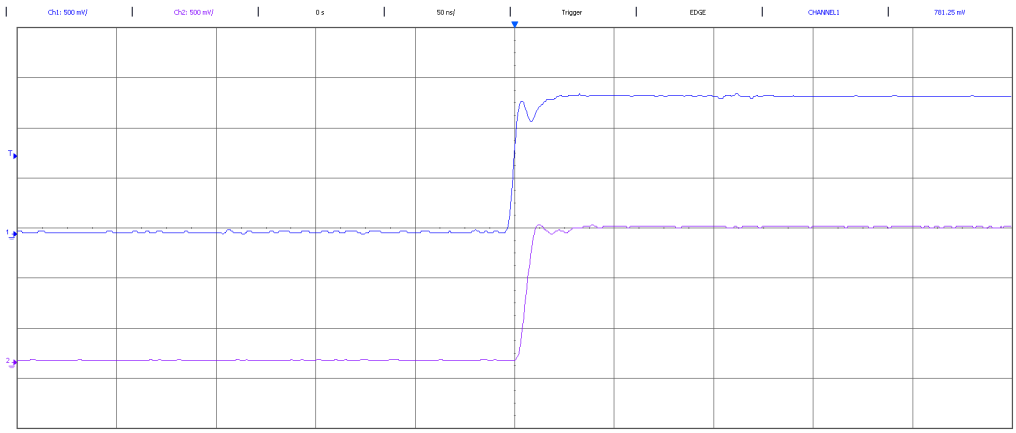

Figure 2.11: Step response of line 7

2.4 Lessons Learned

The message from these "Lenz" experiments is the same as for the Self Induction demonstration: return currents flow as close to their signal path as possible. For a printed circuit board this means that the board layout engineer must provide this nearby return path. Further, it should be noticed from the comparison of traces 5, 6 and 7 in figures 2.9, 2.10 and 2.11 respectively, that it is better to route a trace in the middle of a wide ground plane (trace 6) instead of at the edge of it (trace 5) and still better to also surround the trace by (grounded) guard traces (trace 7).

Chapter 3

Coax Cable

Contents

3.1 Demonstrations on the Coax Board

The Coax Cable Board is an extension of the Lenz' Law Board (see Chapter 2). There we investigated how much of the intended signal reached the end of the interconnection. Here we measure the amount of leakage in a situation where the return path is as close to the signal path as possible.

3.2 Coax Board Views

3.2.1 The Finished Board

The end result of the assembly of the Coax Cable Board is shown in Figure 3.1.

Figure 3.1: The Finished Coax Cable Board.

3.2.2 The Silkscreen

The Silkscreen of the Coax Cable Board shown in Figure 3.2 points out which components should be mounted where:

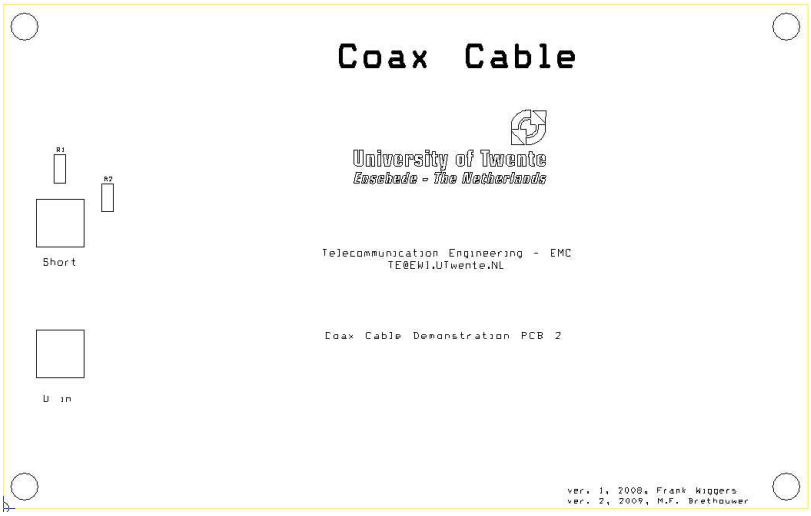

Figure 3.2: The Coax Cable Board Silk Screen.

3.2.3 Bare Board Top View

The etch pattern of the empty board, seen from the top side, is shown in Figure 3.3.

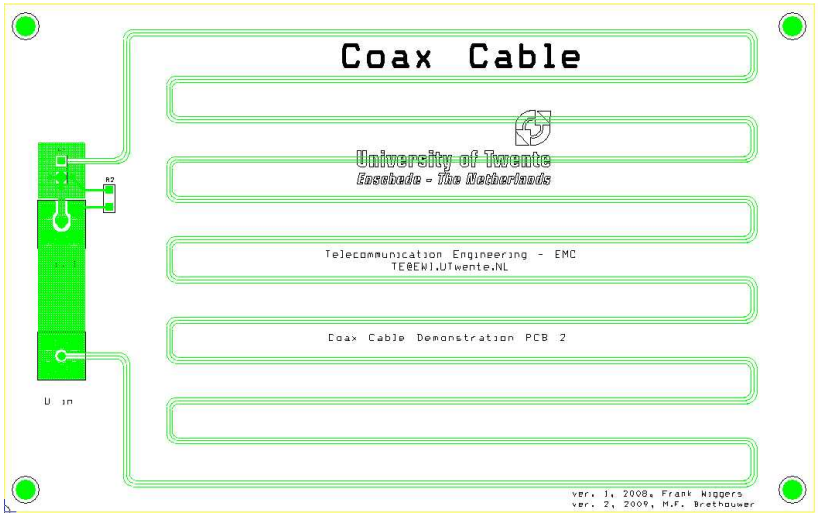

Figure 3.3: The Coax Cable Bare Board (Top View)

3.2.4 Bare Board Bottom View

The etch pattern of the empty board, seen from the bottom side, is shown in Figure 3.4.

Figure 3.4: The Coax Cable Bare Board (Bottom View)

3.2.5 The Board Schematic

The schematic diagram of the Coax board is shown in Figure 3.5.

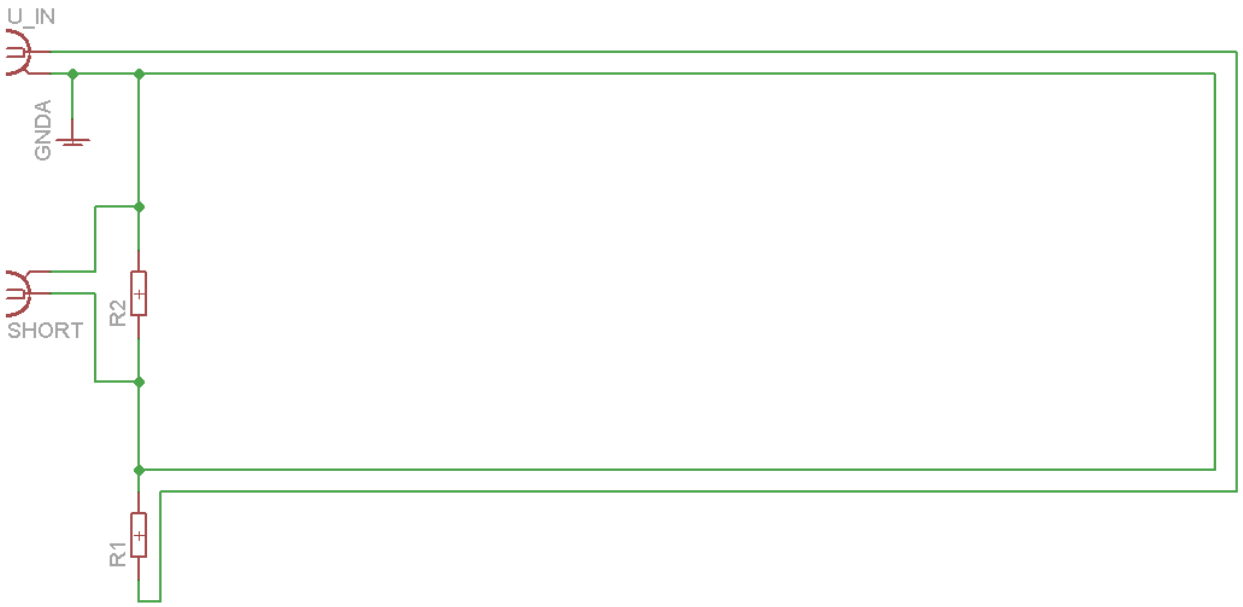

Figure 3.5: The Coax Cable Board Schematic.

3.2.6 The Bill of Materials

The bill of materials of the Coax Cable Board is shown below as Table 3.1.

Table 3.1: Bill of Materials of the Coax Cable Board

REF DES	VALUE	PACKAGE	FOOTPRINT
U in	SMB	SMB	RF/SMB/V
Short	SMB	SMB	RF/SMB/V
R1	51	RESISTOR	SM/R_1206
R2	51	RESISTOR	SM/R_1206

3.3 Board Functional Description

The Coax Cable Board is an extension of the Lenz' Law Board. On the Lenz Board we measured what part of the original source signal arrived at the end of an interconnection. In the Coax Cable Board, the complete return path is laid out close to the signal line. The experiment shows the fraction of the signal current that "leaks out" when a short return path is provided "between the ends" of the coax line. It is connected to a spectrum analyzer with tracking generator as shown for the Transfer Impedance Board in Figure 4.6 on page 31. After calibration of the analyzer-generator combination by directly connecting them, the Coax Cable Board is inserted. The result is shown in Figure 3.6.

If the generator is connected to U in, the Coax Cable demonstration is run in the “Emission” mode (“What leaks out?”). Exchanging the U in and Short connections results in the “Immunity” mode (“What leaks in?”). The result on screen is the same.

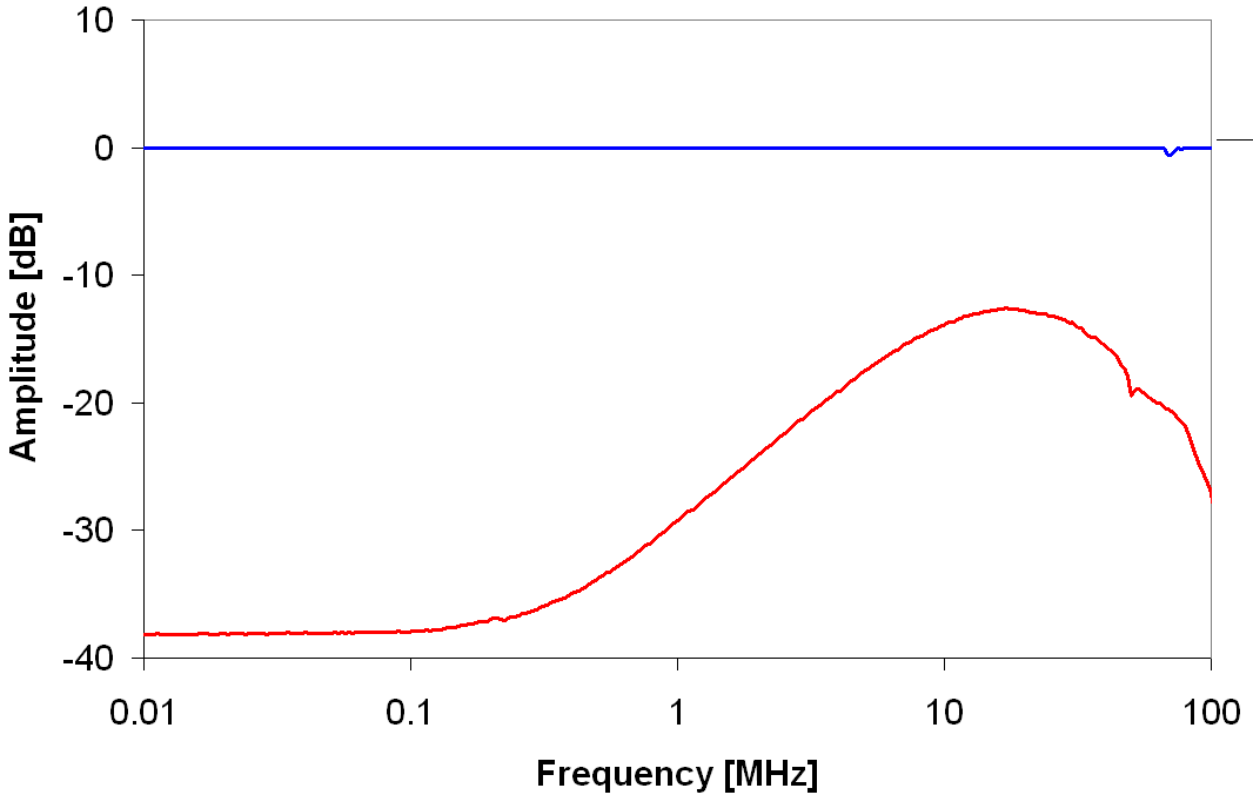

Figure 3.6: Frequency response of the Coax Board (=“Leakage” overe frequency)

3.4 Lessons Learned

As shown in Figure 3.6, the PCB structure we call “Coax” here, leaks energy in the range of 1 to 100 MHz. That means that if other interconnections are routed nearby, usually employing the same return path, increased crosstalk can be expected. The phenomenon is related to Transfer Impedance, described in Chapter 4.
A wide ground plane under the traces would certainly improve the quality of this interconnection.

Chapter 4

Transfer Impedance

Contents

4.1 Demonstrations on the Transfer Impedance Board

Transfer Impedance, for short, Z_T, is a basic property of any interconnection. This board allows the measurement of the Z_T of sample cables.

4.2 Z_T Board Views

4.2.1 The Finished Board

The end result of the assembly of the Z_T Board is shown in Figure 4.1.

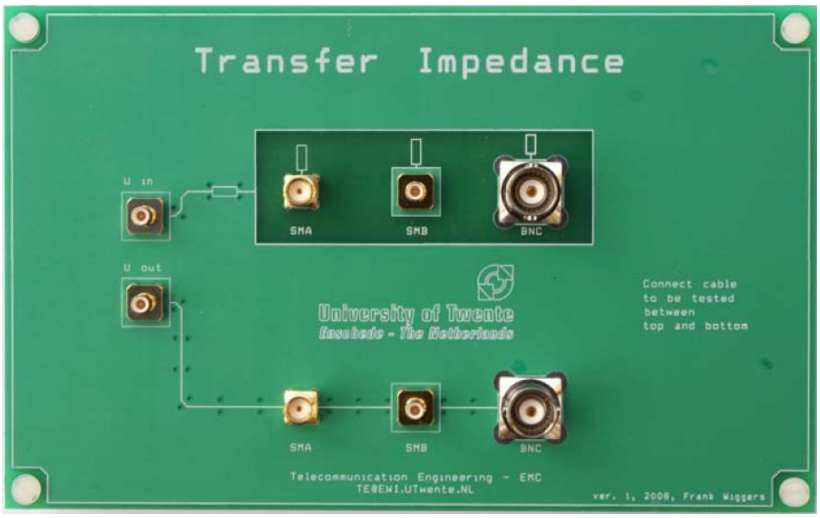

Figure 4.1: The Finished Transfer Impedance Board.

4.2.2 The Silkscreen

The Silkscreen of the Z_T Board shown in Figure 4.2 points out which components should be mounted where:

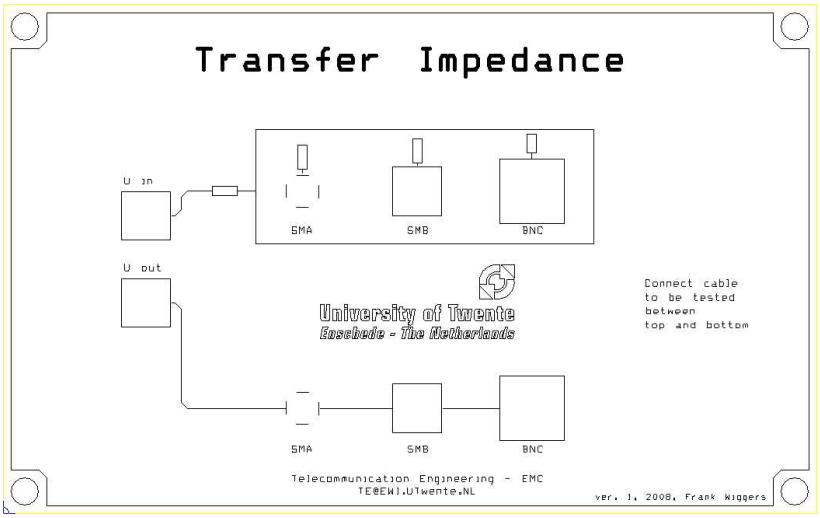

Figure 4.2: The Z_T Board Silk Screen.

4.2.3 Bare Board Top View

The etch pattern of the empty board, seen from the top side, is shown in Figure 4.3.

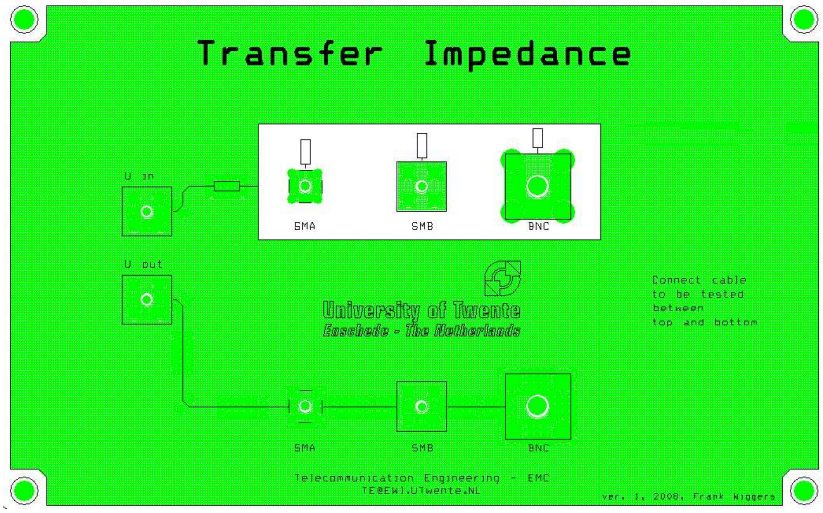

Figure 4.3: The Z_T Bare Board (Top View)

4.2.4 Bare Board Bottom View

The etch pattern of the empty board, seen from the bottom side, is shown in Figure 4.4.

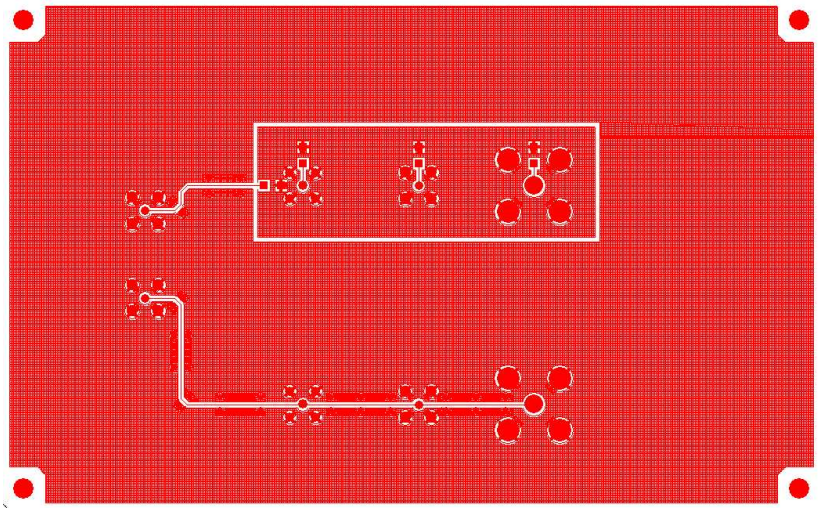

Figure 4.4: The Z_T Bare Board (Bottom View)

4.2.5 The Board Schematic

The schematic diagram of the Z_T board is shown in Figure 4.5.

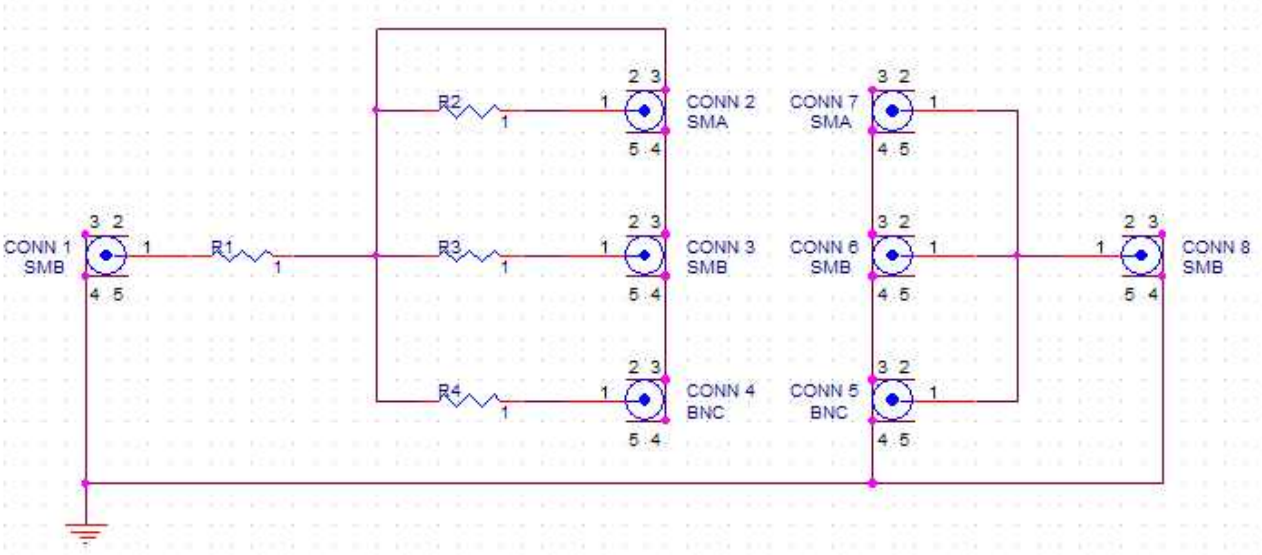

Figure 4.5: The Transfer Impedance Board Schematic.

4.2.6 The Bill of Materials

The bill of materials of the Z_T Board is shown below as Table 4.1.

Table 4.1: Bill of Materials of the Z_T Board

REF DES	VALUE	PACKAGE	FOOTPRINT
SMB 1	SMB	SMB	SMB_JACK
SMB 2	SMB	SMB	SMB_JACK
CONN 4	SMB	SMB	RF/SMB/V
CONN 5	SMB	SMB	RF/SMB/V
INPUT	SMB	SMB	RF/SMB/V
OUTPUT	SMB	SMB	RF/SMB/V
R1	1	RESISTOR	SM/R_1206
R2	1	RESISTOR	SM/R_1206
R3	1	RESISTOR	SM/R_1206
R4	1	RESISTOR	SM/R_1206
SMA 1	SMB	SMB	RF/SMA/V
SMA 2	SMB	SMB	RF/SMA/V

4.3 Board Functional Description

This board has provisions to test the transfer impedance of cables as function of frequency. For that purpose a spectrum analyzer with tracking generator is used. A cable specimen is connected between two two opposite sets of connectors, labeled “SMA”, “SMB” or “BNC” on the board. If you have ordered bare boards, you could mount other types of coax connectors. The spectrum analyzer is calibrated by connecting the tracking generator output directly to the input to indicate “0 dB” over the entire selected frequency range. Then, the transfer impedance board with the cable under test is inserted as shown in Figure 4.6. The generator signal conductor is connected through a small resistor to an insulated ground plane “island” on which the first connector for the cable under test is terminated. The signal conductor of this cable is also connected (shorted) to this same point with a small resistor. The generator return conductor is connected to the other end of the return conductor of the cable under test. In this way, a “noise” current is fed over the tested cable return. The analyzer input is connected to the second end of the cable under test to measure the differential mode signal that is generated on the cable under test. A frequency up to 50 or 100 MHz is appropriate. The

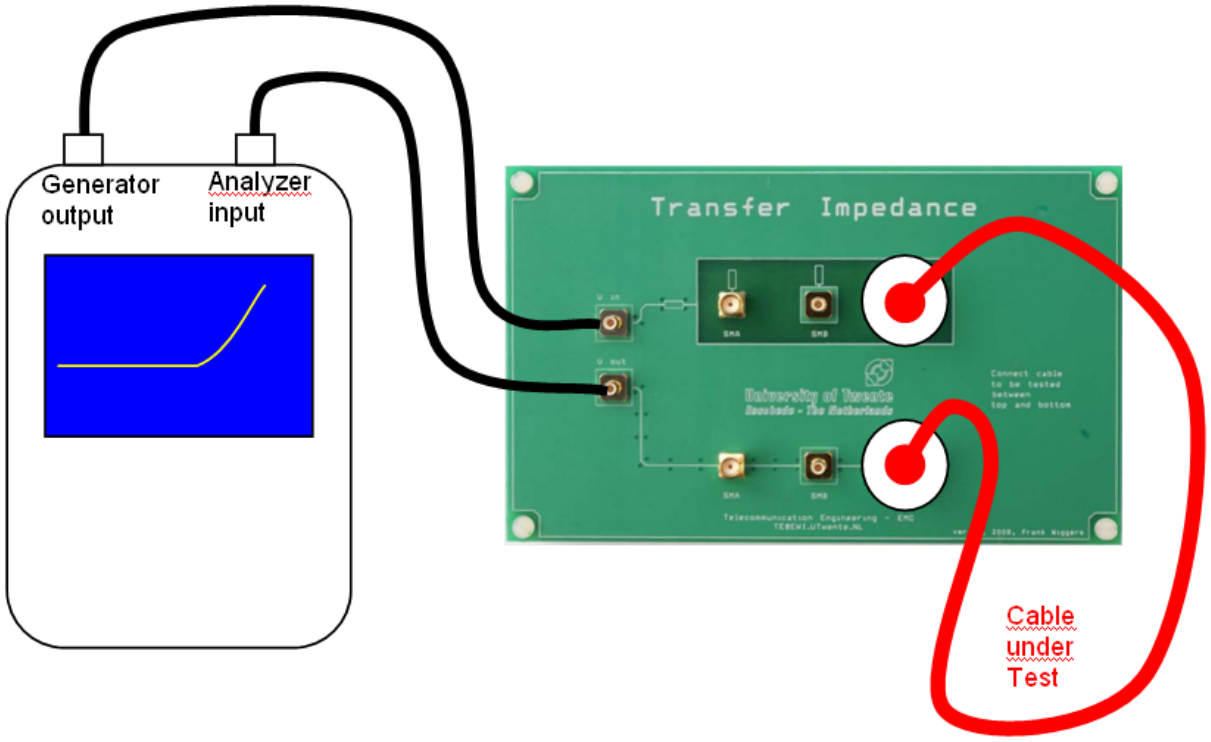

Figure 4.6: Connection Diagram of the Transfer Impedance Board

lowest frequency is determined by the analyzer. A sample of measurement results is shown in Figure 4.7. The way the demonstration is set up, the immunity aspect of the cable under test is measured. To demonstrate the opposite emission aspect, the connections of the tracking generator output and spectrum analyzer input should be exchanged.

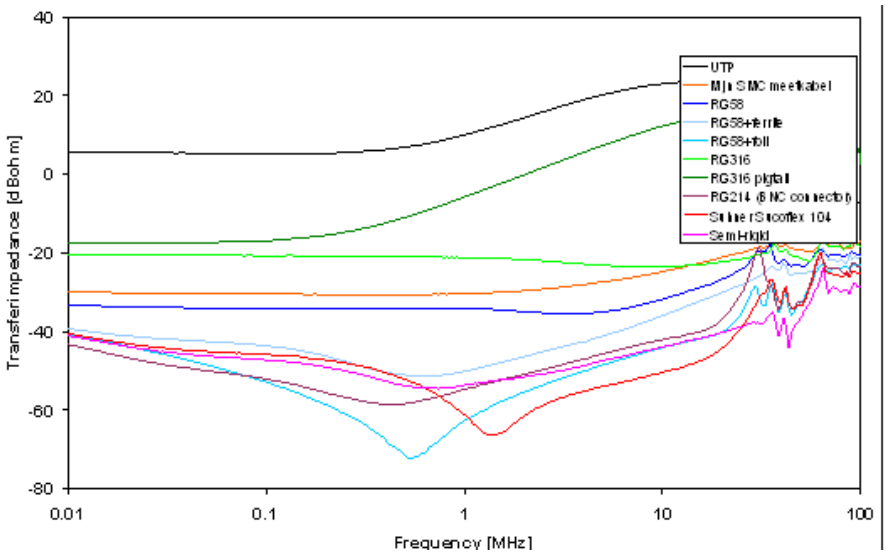

Figure 4.7: Some Examples of Cable Transfer Impedances with Frequency

4.4 Lessons Learned

The "Z_T" experiments show that:

1. Cables generate differential mode noise voltages due to (are susceptible to) noise currents through their return conductors.
2. Cables generate (emit) common mode currents through their return conductors due to differential mode signals flowing in them.
3. If the cable shield is thick enough, the skin effect helps to reduce the transfer impedance even further in parts of the frequency spectrum.
4. Developers should specify the required transfer impedance for their cable designs over the relevant frequency range.

Chapter 5

Crosstalk Basic Phenomena

Contents

5.1 Demonstrations on the Crosstalk Basic Phenomena Board

The Crosstalk Basic Phenomena Board illustrates the mutual inductance and capacitance effect underlying crosstalk. Further it is shown that there is a ceiling to the amount of crosstalk and that the level of this ceiling is set by designable board layout parameters.

5.2 Crosstalk Basic Phenomena Board Views

5.2.1 The Finished Board

The end result of the assembly of the Crosstalk Basic Phenomena Board is shown in Figure 5.1

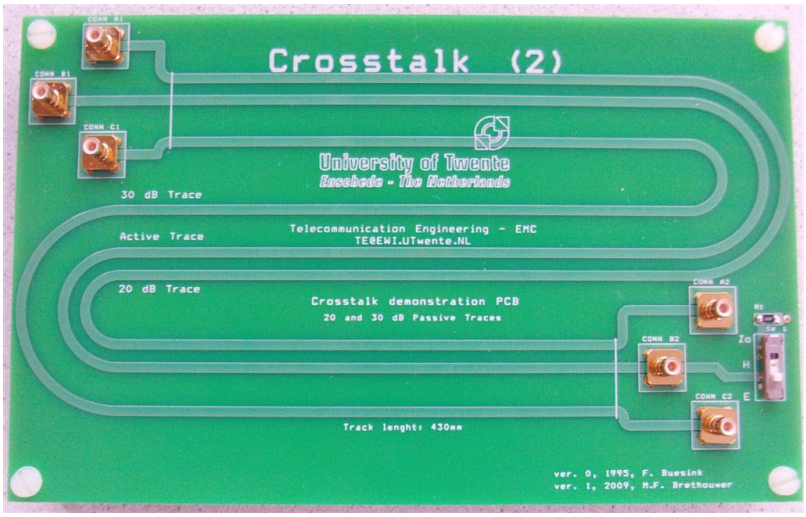

Figure 5.1: The Finished Crosstalk Basic Phenomena Board.

5.2.2 The Silkscreen

The Silkscreen of the Crosstalk Basic Phenomena Board shows where which components should be mounted:

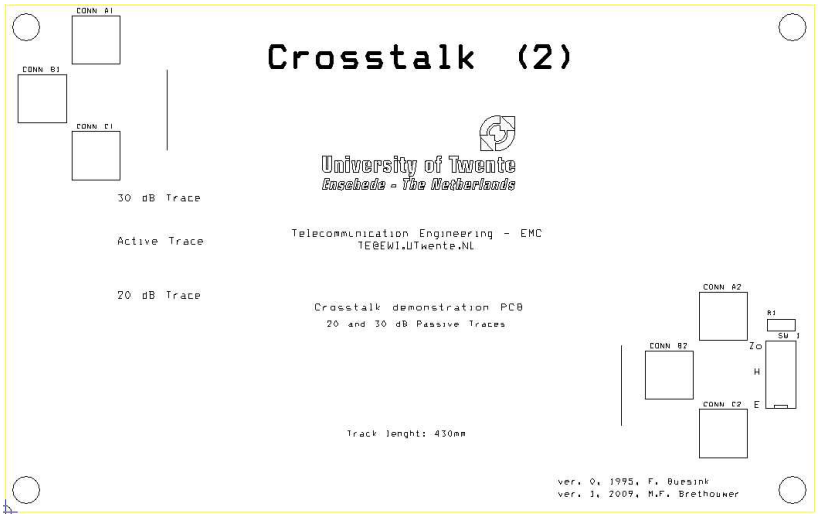

Figure 5.2: The Crosstalk Basics Board Silk Screen.

5.2.3 Bare Board Top View

The etch pattern of the empty board, seen from the top side, is shown in Figure 5.3.

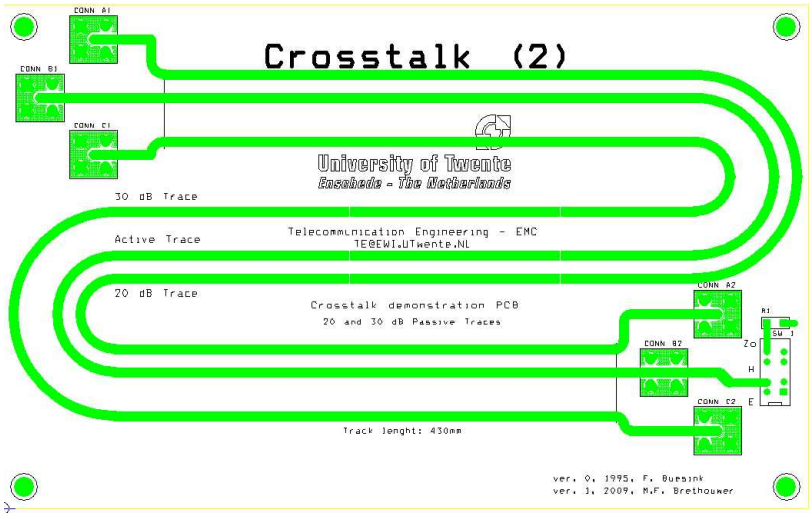

Figure 5.3: The Crosstalk Basics Bare Board (Top View)

5.2.4 Bare Board Bottom View

The etch pattern of the empty board, seen from the bottom side, is shown in Figure 5.4.

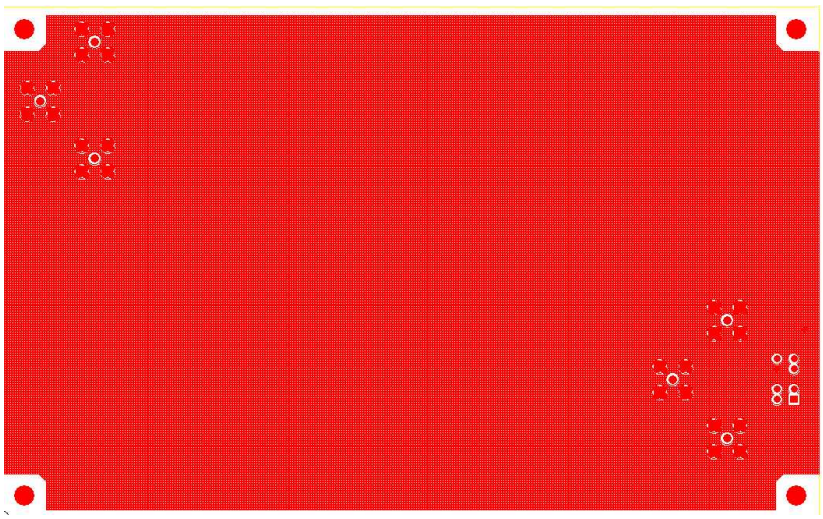

Figure 5.4: The Crosstalk Basics Bare Board (Bottom View)

5.2.5 The Board Schematic

The schematic diagram of the Crosstalk Basic Phenomena Board is shown in Figure 5.5

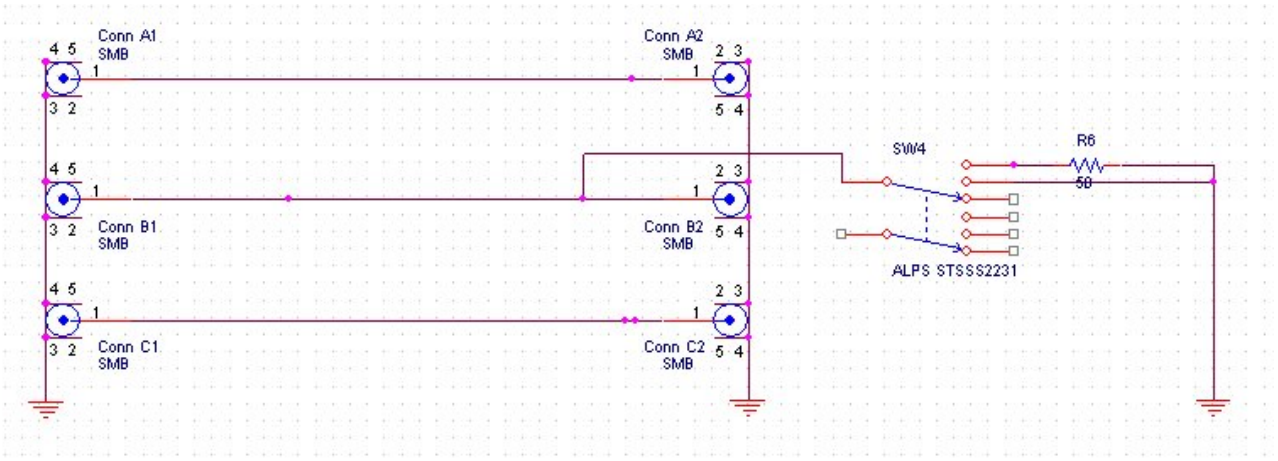

Figure 5.5: The Crosstalk Basics Board Schematic.

5.2.6 The Bill of Materials

The components to complete the Crosstalk Basic Phenomena Board are shown in Table 5.1.

Table 5.1: Bill of Materials of the Crosstalk Basic Phenomena Board

REF DES	VALUE	PACKAGE	FOOTPRINT
CONN A1	SMB	SMB	RF/SMB/V
CONN B1	SMB	SMB	RF/SMB/V
CONN C1	SMB	SMB	RF/SMB/V
CONN A2	SMB	SMB	RF/SMB/V
CONN B2	SMB	SMB	RF/SMB/V
CONN C2	SMB	SMB	RF/SMB/V
SW 1	3 pos DP	DP/3	ALPS-STSSS2231
R1	51	RESISTOR	SM/R_1206

5.3 Board Functional Description

The “Crosstalk Basic Phenomena” Board can be operated both in the time and frequency domain. The middle trace on the demo board, the active trace, transmits a signal from either a square wave generator or from a tracking generator of a spectrum analyzer. The active trace load can be switched from “characteristic termination” to “open ended” or ”short circuited”. Depending on the

position of the switch, the active line end will or will not reflect the signals on that line. The effects (crosstalk) on the passive lines can be observed at both the near end (closest to the signal generator) and the far end (near the active line termination switch). Two passive lines have been routed. They have been labeled as a “20 dB trace” and a “30 dB trace” respectively. To see the difference, a spectrum analyzer with tracking generator is used. The frequency span should be at least 200 MHz, preferably 400 MHz (starting, say, at 1 MHz). The connection diagram in Figure 5.6 shows the details for measuring the “20 dB line”. To measure the “30 dB line”, the Spectrum Analyzer input line is now connected to “CONN C1” and the 50Ω load is transferred to “CONN C2”. The results

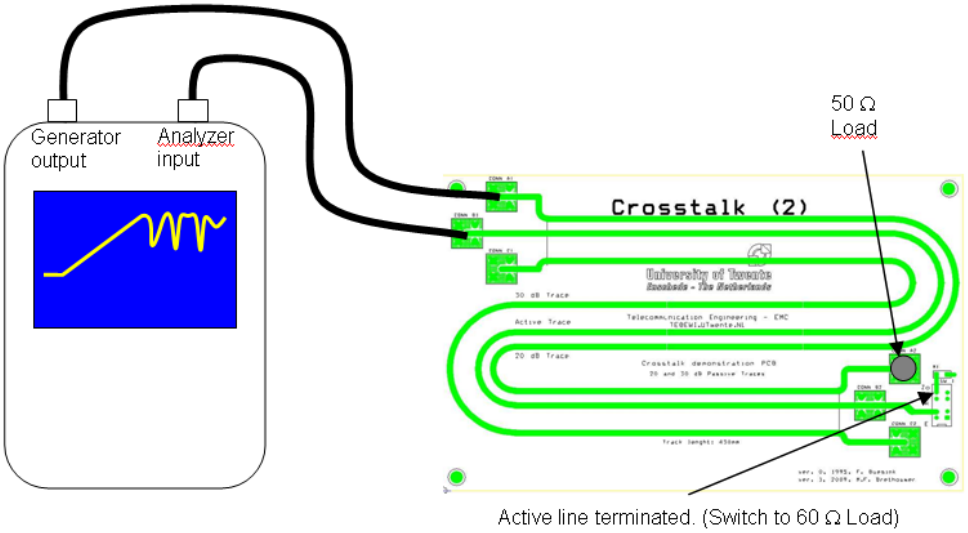

Figure 5.6: The Crosstalk Basics Connection Diagram using a Spectrum Analyzer with Tracking Generator

of measurements of the 20 and 30 dB passive traces are shown in Figure 5.7. In both cases, the active line is terminated with a resistor, R1, between 50 and 60 Ohms (switch SW 1 in the “Zo” position). An interesting phenomenon is the sharp decline in crosstalk on both the 20 and 30 dB lines at almost 200 MHz. This appears to be the frequency at which $\frac{\lambda}{2}$ exactly fit the trace. Dr. Howard Johnson calls this frequency the “critical frequency” in his book “High Speed Digital Design”. This sharp decline in crosstalk repeats at higher frequencies (at multiples of $\frac{\lambda}{2}$. A more practical effect, however is that there is a maximum crosstalk level. Figure 5.7 shows two of them at 100 and 300 MHz, frequencies at which $\frac{\lambda}{4}$ and $\frac{3\lambda}{4}$. If these maxima are interconnected with an imaginary line, an asymptote is found. The level at which this asymptote lies, depends on the distance between the active and passive lines. For this board, the two passive traces were designed to have a maximum crosstalk level of -20 and -30 dB respectively. Whether these levels are reached depends on the frequency spectrum of the source connected to the active trace. To see the effects of an unterminated source/active line in the frequency domain, the switch SW 1 can be set to “H” (middle position, active line is shorted to ground at the switch) or to “E” (bottom position, active line is open circuit at the switch). The results are shown in Figure 5.8 for the “20 dB passive line” and in Figure 5.9 for the “30 dB passive line”. The passive lines were terminated in 50Ω in both situation. While measuring the 30 dB line, an experiment can be added by terminating the 20 dB line on one or both sides. That will show the influence of a more or less floating line near the active line. If desired, any of the passive lines can be used as active line, using the other two to monitor crosstalk. The experiment described above measures crosstalk at the near end. By exchanging the position of the 50Ω load

and the spectrum analyzer input, the characteristics of the far end crosstalk can be explored.

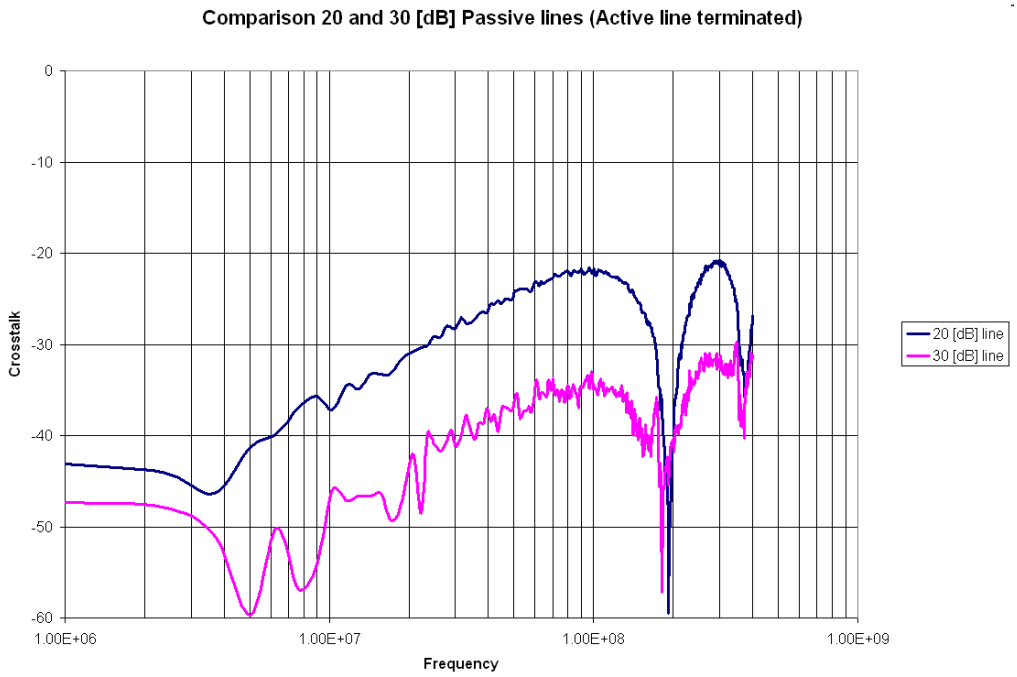

Figure 5.7: Comparison of Crosstalk on 20 and 30 [dB] lines. Active line terminated

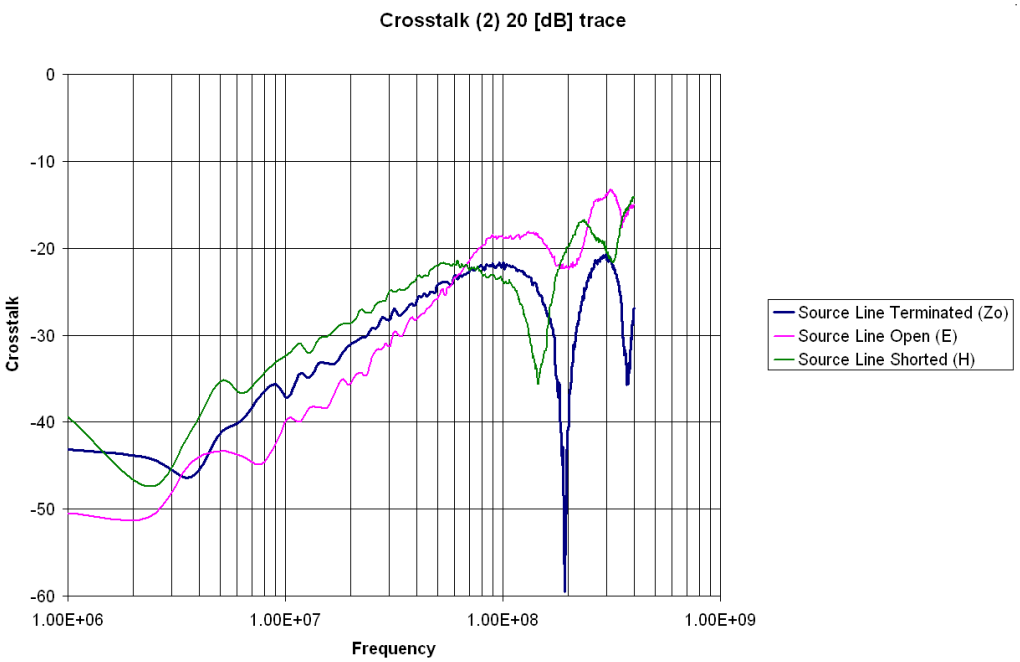

Figure 5.8: Crosstalk on 20 dB line. Active line terminated, open and shorted

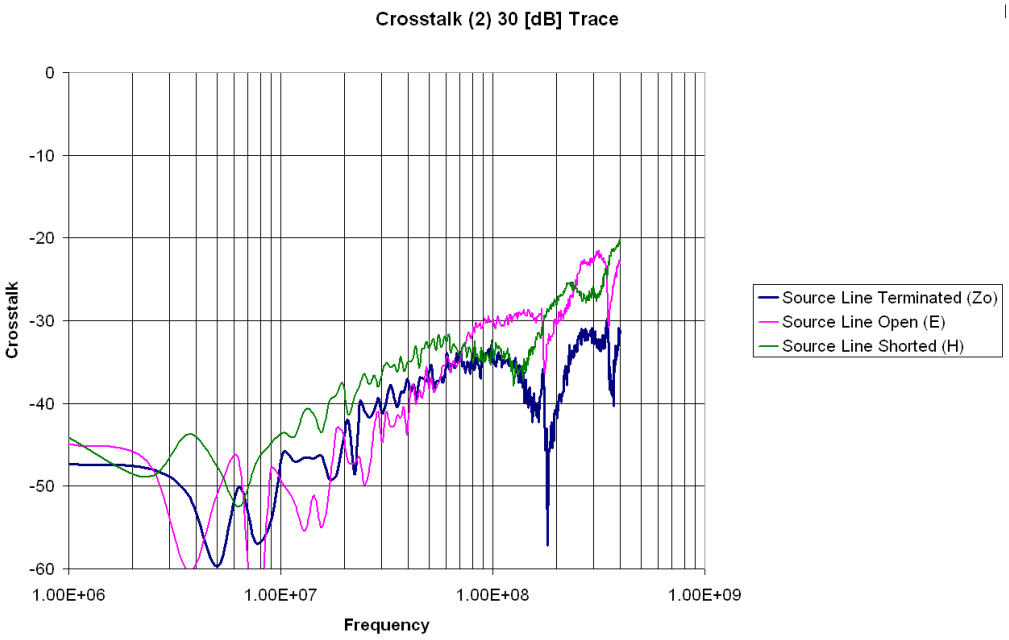

Figure 5.9: Crosstalk on 30 dB line. Active line terminated, open and shorted

5.4 Lessons Learned

The "Crosstalk Basic Phenomena" experiments show that:

1. Crosstalk features three aspects, best shown in the frequency domain:
   (a) A low frequency "$I \cdot R$" resistive effect. This is a frequency independent section which can be safely neglected in most cases.
   (b) Crosstalk increasing proportional with frequency based on inductive and capacitive effects.
   (c) A "Transmission Line Effects" section where the line lengths are longer than $\frac{1}{4} \cdot \lambda$. The horizontal asymptote in this range of frequencies is independent of frequency. The level of crosstalk is determined by the geometry of the cross sections of the signal lines involved. These geometries are essentially designable parameters that can be set by the lay-out engineer. Per unit length line capacitance, inductance and inter-line capacitance and mutual inductance are parameters that play an important role.
2. Given the geometry of the PCB traces and surrounding ground (or power) planes, a maximum level exists for crosstalk in the "Transmission-Line" frequency range. The line termination impedances are important here. The asymptotic crosstalk ceiling is lowest if the active trace is characteristically terminated. Reflections on the active line increase the perceived crosstalk level.
3. Crosstalk in the "Transmission-Line Frequency Range" reaches the asymptotic level only if the signal frequencies transmitted contain these frequencies.
4. In the time-domain, a distinct difference between forward and backward crosstalk can be observed if the line is considerably longer than the "Length of the Leading Edge". Forward crosstalk has a duration equal to the rise or fall time of the signal on the active trace. The backward crosstalk in addition has the duration of twice the propagation delay over the total length where the lines crosstalk.
5. When reflections occur on the active signal trace, backward crosstalk can be observed at both ends of the passive line. The only way to avoid backward crosstalk (on the far end of the line) is to characteristically terminate the active signal line. Note that in many digital designs, lines can be passive or active depending on the state of the system.

Chapter 6

Crosstalk Layout Issues

Contents

6.1 Demonstrations on the Crosstalk Layout Issues Board

The Crosstalk Layout Issues Board focusses on common layout mistakes that may have profound effects on the amount of crosstalk experienced between PCB interconnections.

6.2 Crosstalk Layout Issues Board Views

6.2.1 The Finished Board

The end result of the assembly of the Crosstalk Layout Issues Board is shown in Figure 6.1

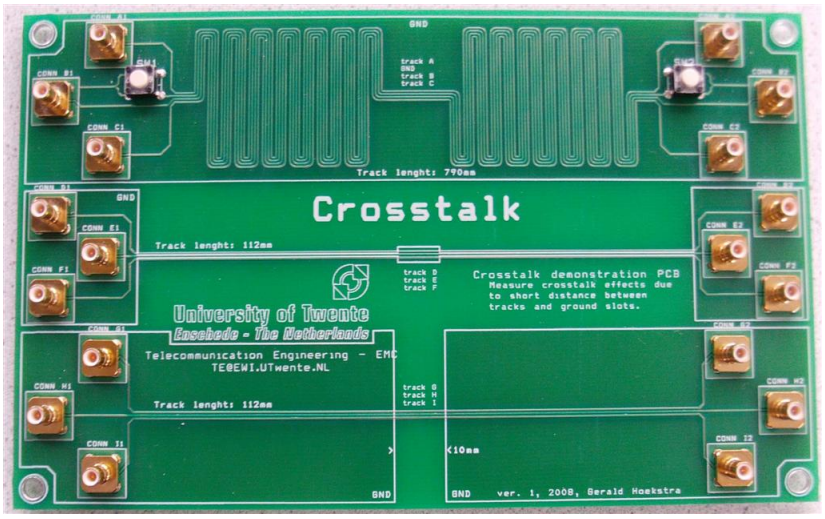

Figure 6.1: The Finished Crosstalk Layout Issues Board.

6.2.2 The Silkscreen

The Silkscreen of the Crosstalk Layout Issues Board shows where which components should be mounted:

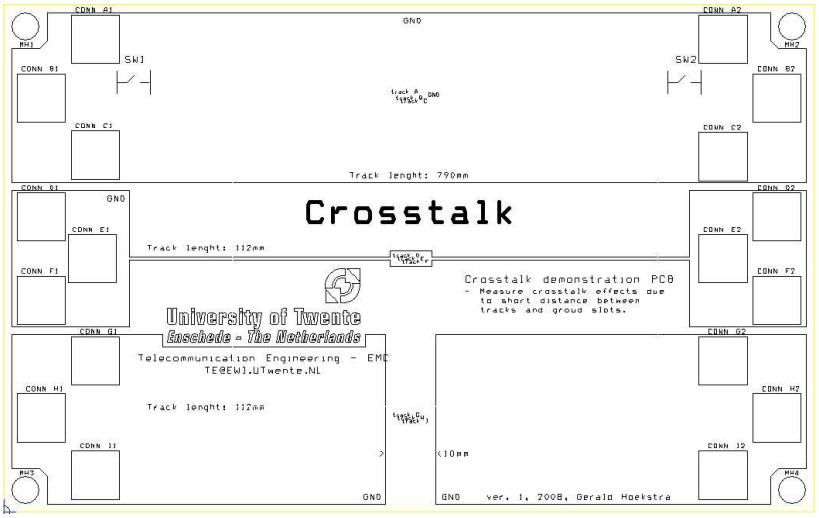

Figure 6.2: The Crosstalk Layout Issues Board Silk Screen.

6.2.3 Bare Board Top View

The etch pattern of the empty board, seen from the top side, is shown in Figure 6.3.

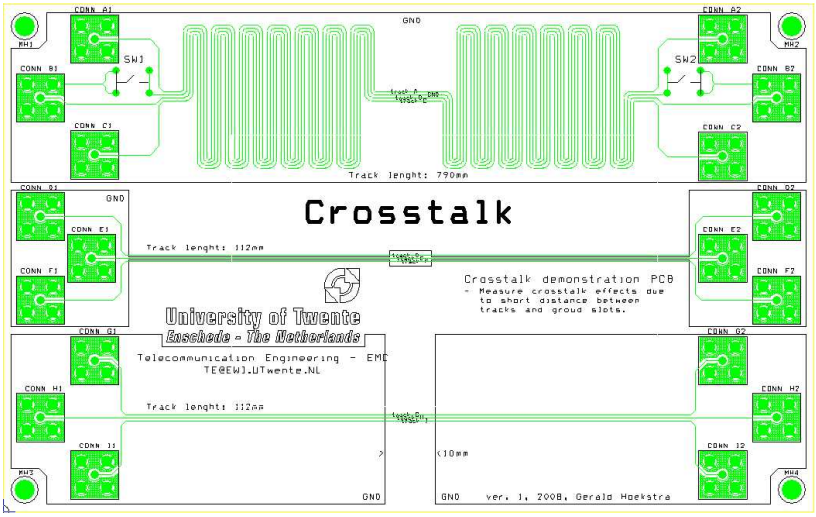

Figure 6.3: The Crosstalk Layout Issues Bare Board (Top View)

6.2.4 Bare Board Bottom View

The etch pattern of the empty board, seen from the bottom side, is shown in Figure 6.4.

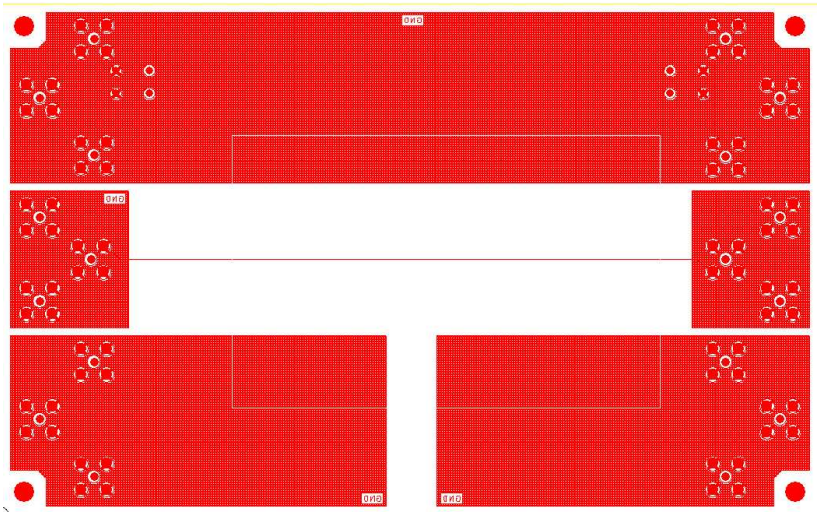

Figure 6.4: The Crosstalk Layout Issues Bare Board (Bottom View)

6.2.5 The Board Schematic

The schematic diagram of the Crosstalk Layout Issues Board is shown in Figure 6.5

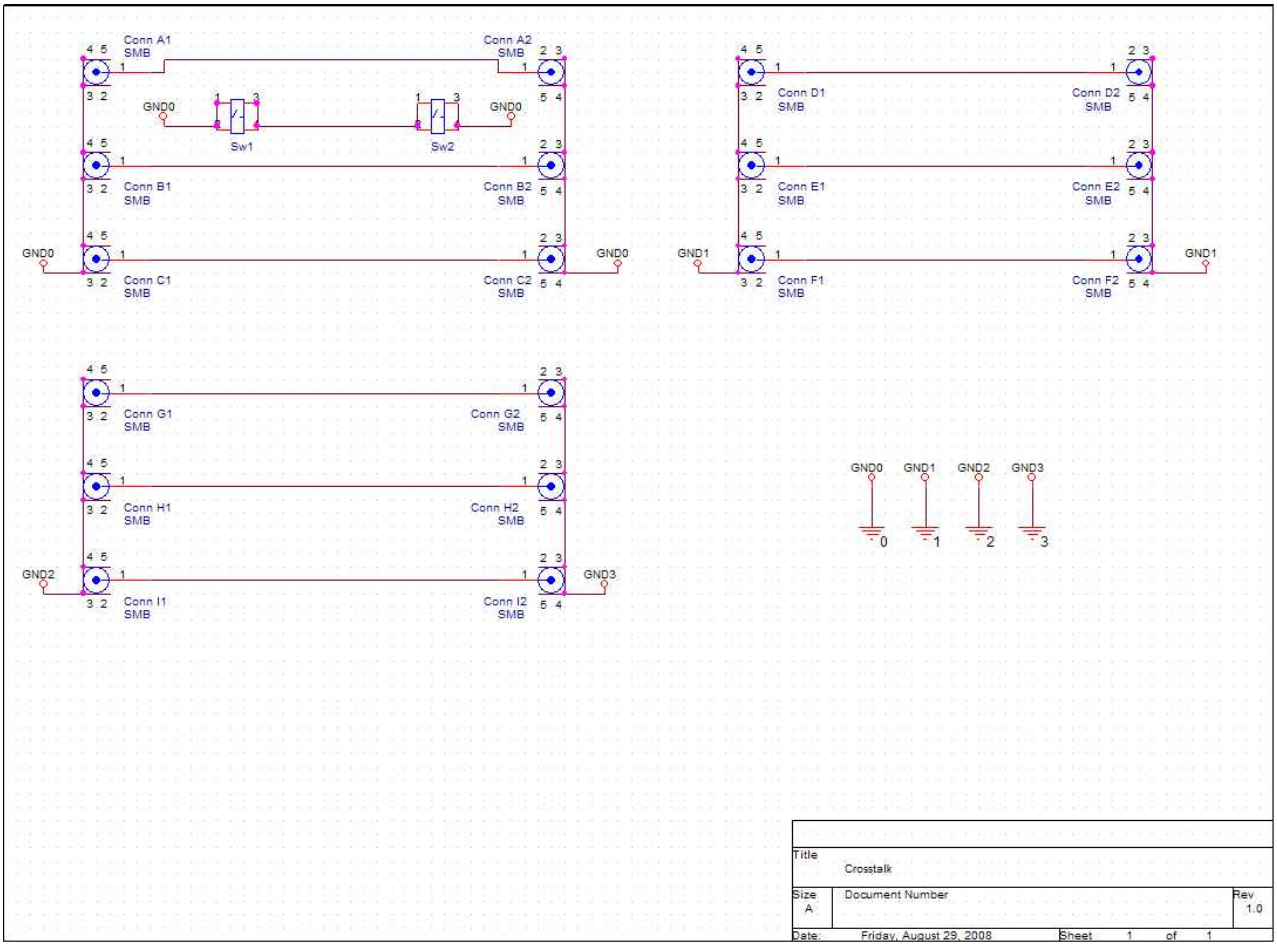

Figure 6.5: The Crosstalk Layout Issues Board Schematic.

6.2.6 The Bill of Materials

The components to complete the Crosstalk Layout Issues Board are shown in Table 6.1.

Table 6.1: Bill of Materials of the Crosstalk Layout Issues Board

REF DES	VALUE	PACKAGE	FOOTPRINT
CONN A1	SMB	SMB	RF/SMB/V
CONN B1	SMB	SMB	RF/SMB/V
CONN C1	SMB	SMB	RF/SMB/V
CONN A2	SMB	SMB	RF/SMB/V
CONN B2	SMB	SMB	RF/SMB/V

Table 6.1: Bill of Materials of the Crosstalk Layout Issues Board (cont'd)

REF DES	VALUE	PACKAGE	FOOTPRINT
CONN C2	SMB	SMB	RF/SMB/V
CONN D1	SMB	SMB	RF/SMB/V
CONN E1	SMB	SMB	RF/SMB/V
CONN F1	SMB	SMB	RF/SMB/V
CONN D2	SMB	SMB	RF/SMB/V
CONN E2	SMB	SMB	RF/SMB/V
CONN F2	SMB	SMB	RF/SMB/V
CONN G1	SMB	SMB	RF/SMB/V
CONN H1	SMB	SMB	RF/SMB/V
CONN I1	SMB	SMB	RF/SMB/V
CONN G2	SMB	SMB	RF/SMB/V
CONN H2	SMB	SMB	RF/SMB/V
CONN I2	SMB	SMB	RF/SMB/V
SW1	CON4_8	CON4_9	SWITCH-4PIN-TYCO-FSM4JH
SW2	CON4_8	CON4_9	SWITCH-4PIN-TYCO-FSM4JH

6.3 Board Functional Description

The "Crosstalk Layout Issues" Board is best operated in the frequency domain. It has three distinct sections that can be operated independently. The first section, between connectors A1-A2, B1-B2 and C1-C2 has trace lengths around 790 mm, routed over a wide ground plane. This implies a critical frequency of around 120 MHz (where $\frac{\lambda}{2}$ fits the length of the trace). The other two sections, between connectors D1-D2, E1-E2 and F1-F2 or between connectors G1-G2, H1-H2 and I1-I2 are 112 [mm] long with a corresponding critical frequency of 860 MHz. For a short explanation of the critical frequency, see the description in Section 5.3 on page 38. Starting with the long traces at the top of the board, there are three traces with an additional ground (or "guard") trace between the traces A1-A2 and B1-B2. Any trace could be used as an active trace, but the trace between CONN B1 and CONN B2 is used as the active trace for this example. The guard trace is connected when both switches SW1 and SW2 are pressed. The spectrum analyzer is connected as shown in Figure 6.6. The results of the measurements are shown in Figure 6.7. Assuming the active signal on connector B1 and measuring the crosstalk on connector A1, four situations are shown in Figure 6.7. The dark blue line "B1 to A1 Guard Floating" is the situation where the guard trace is not connected on either side. The asymptote, reached around 100 MHz lies at approximately 10 dB under the level of the active line (0 dB in the graph). When both switches are pressed, the red line "B1 to A1 SW1 & SW2 closed" is measured. It is interesting to notice that only the "Low Frequencies" (below 100 MHz) are affected (12 dB or a factor of 4 less). In the higher frequencies, the asymptote still lies around -10 [dB]. If only one of the two switches is closed, the purple "B1 to A1 SW1 closed" and green "B1 to A1 SW2 closed" lines are found. Both a little worse than the original "B1 to A1 Guard Floating". The extra peaks at 50 MHz are formed because at that frequency the guard trace resonates and in fact increases the crosstalk! The measurement "B1 to C1 Guard Floating" (orange

line) is added to show the crosstalk for two traces at the normal trace separation distance in this A B C group. The high frequency asymptote lies at -8 dB. The middle section of the board has three traces routed close together between two groups of connectors D1, E1 and F1 on the left hand side to D2, E2 and F2 at the right hand side. Both connector groups are placed on local ground planes. Under the traces there is no ground plane but only a thin ground trace connecting these local planes (same width as the signal traces). The board is connected as in Figure 6.6 only the signal source is connected to CONN D1, the start of the active trace for this group. The 50Ω load is placed on CONN D2. Crosstalk in then measured on traces E1 - E2 and F1 - F2 respectively. The results are shown in Figure 6.8 as “D1 to E1 no SW” (blue line) and “D1 to F1 no SW” (red line). The crosstalk between lines E1 - E2 and F1 - F2 is identical to that between D1 - D2 and E1 - E2. Finally, the bottom section of the board with lines between connectors G, H and I, is explored. On the bottom of the board a wide ground plane is placed between the two connector groups. But there is a gap in this ground plane of about 10 mm and these two half planes are connected nowhere. Using the spectrum analyzer - tracking generator combination again, it is connected to CONN H1 (tracking generator) and CONN G1 (Spectrum Analyzer) with 50Ω loads on the corresponding CONN H2 and CONN G2. The crosstalk measured is shown in Figure 6.9. As the two ground plane sections on the board are not connected, the ground connection is now via the connectors of the spectrum analyzer tracking generator! This creates a huge ground loop. That is reflected in the crosstalk which now extends all the way to the low frequency border of the graph in Figure 6.9!

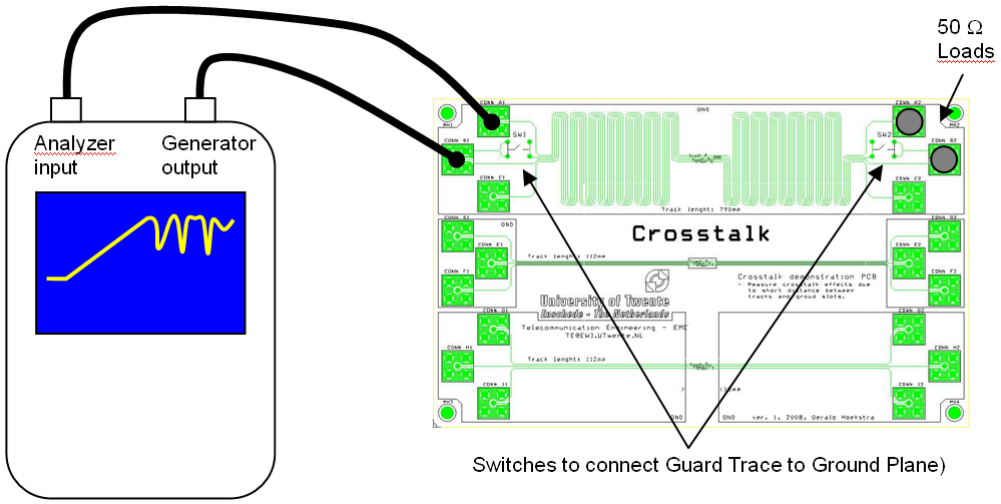

Figure 6.6: The Crosstalk Layout Issues Connection Diagram using a Spectrum Analyzer with Tracking Generator

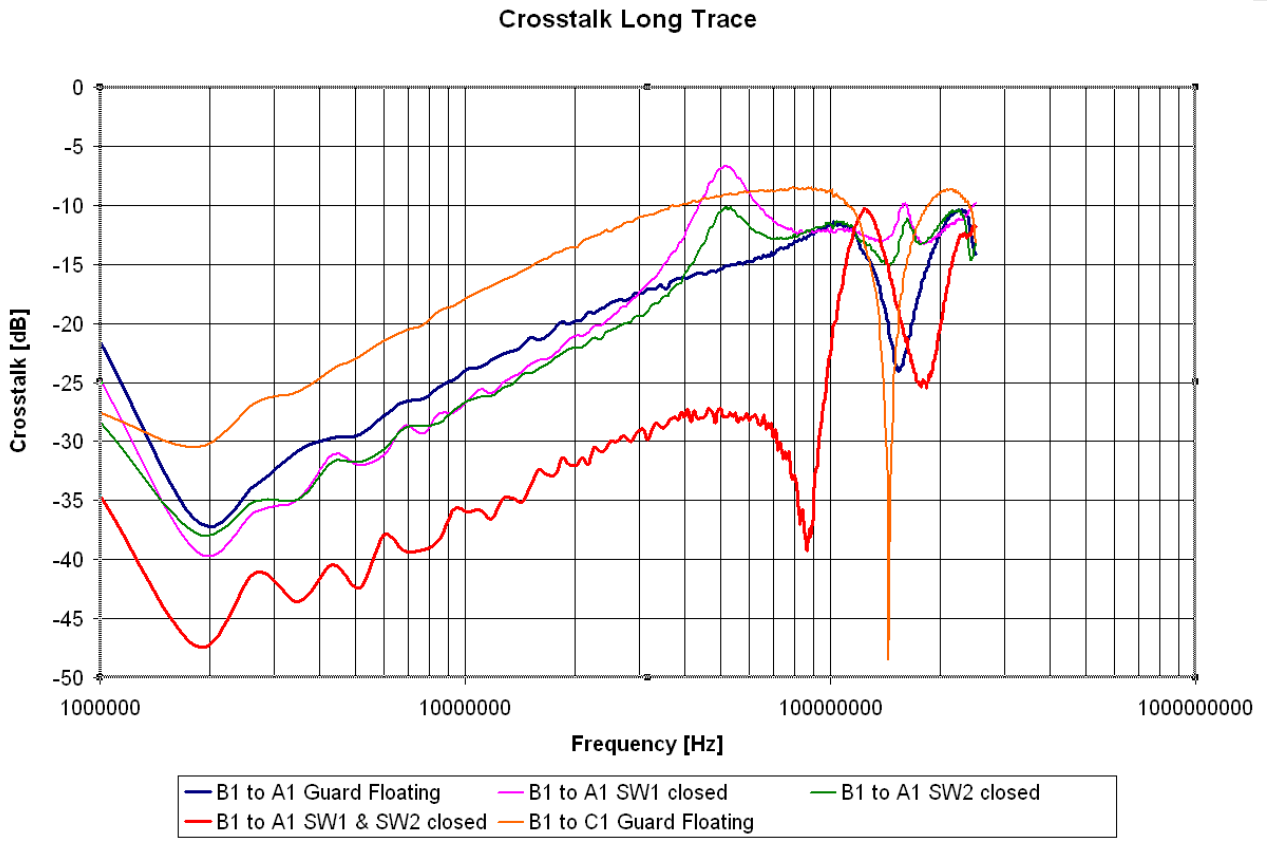

Figure 6.7: Frequency Response of crosstalk from line B to lines A and C

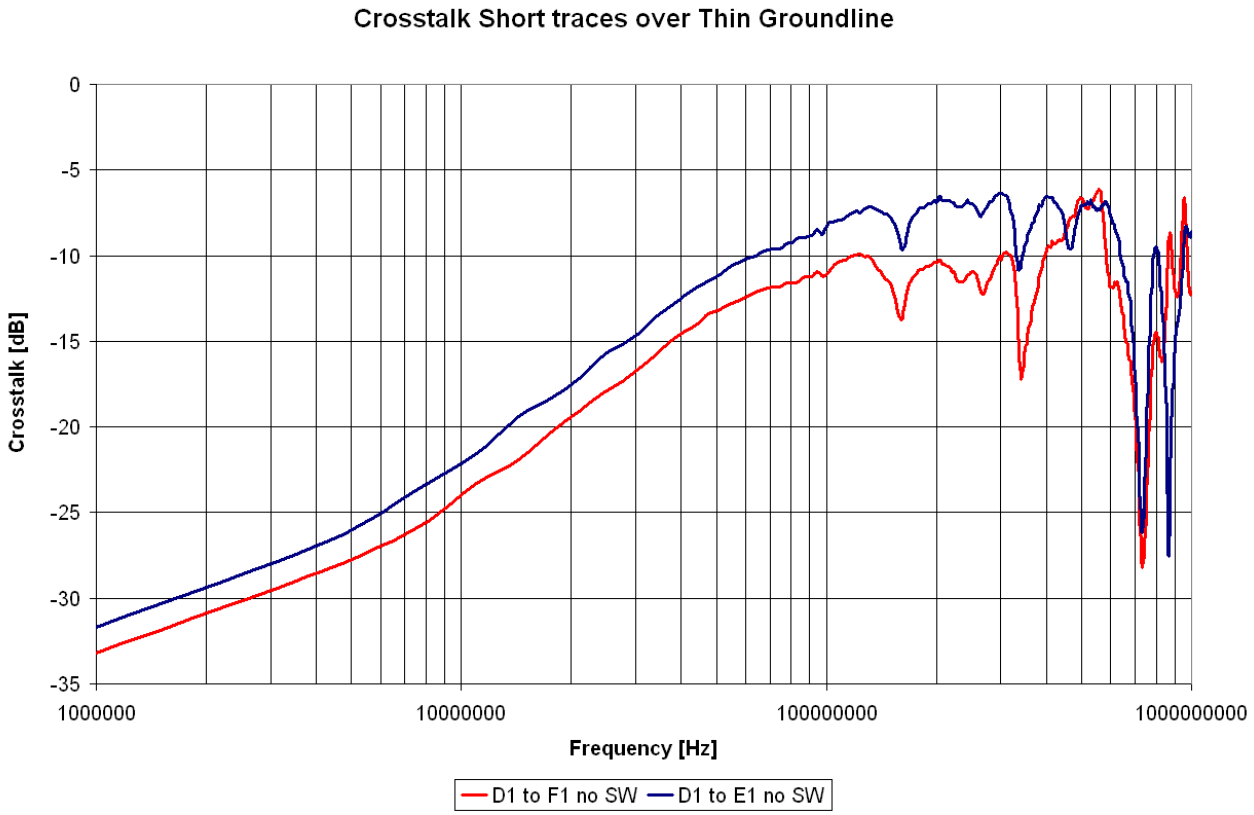

Figure 6.8: Crosstalk between combinations of lines D, E and F

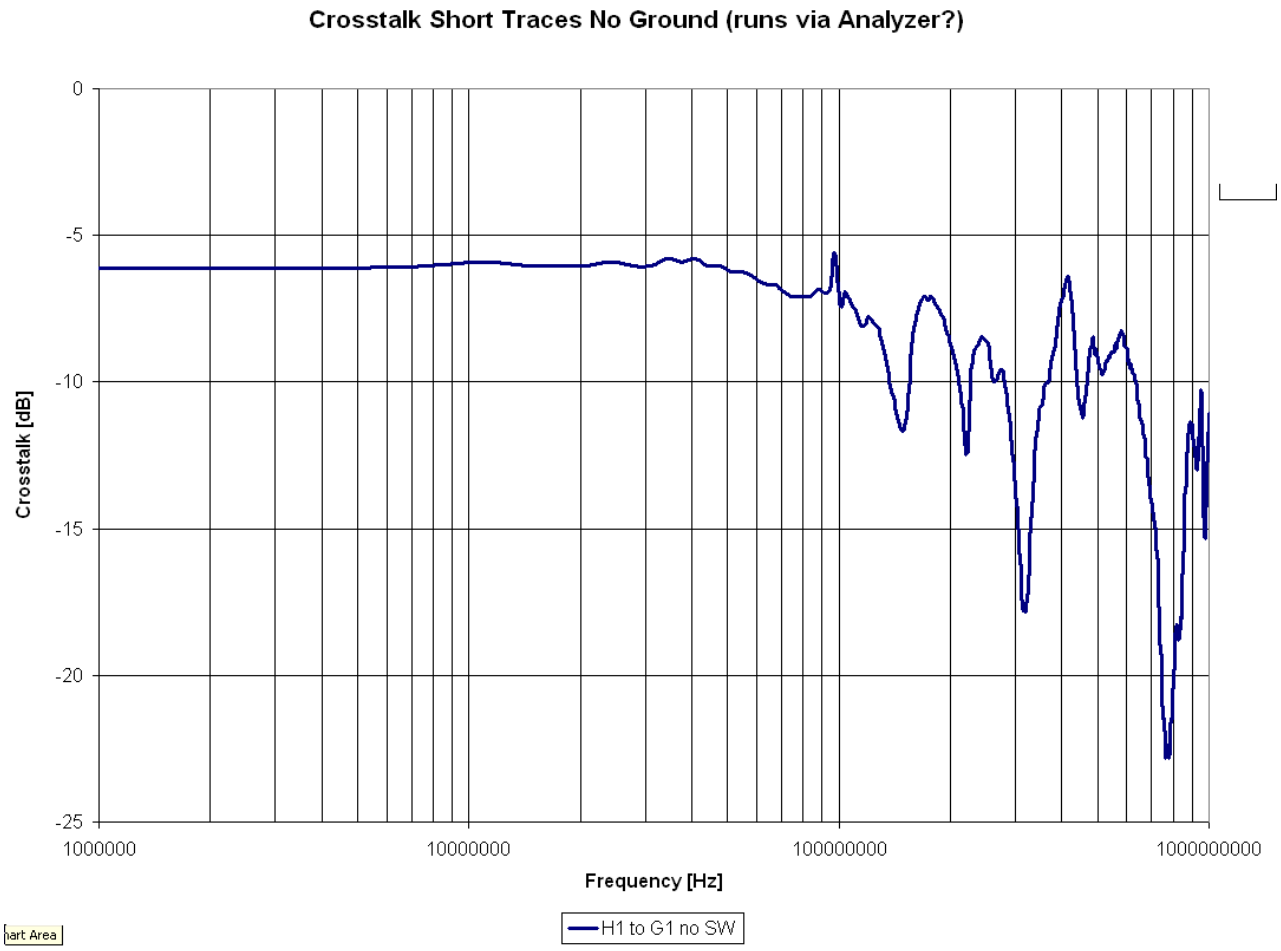

Figure 6.9: Crosstalk between lines H and G

6.4 Lessons Learned

The “Crosstalk Layout Issues” experiments show that:

1. Guard traces (a grounded trace between two adjacent signal traces) can help to reduce crosstalk only below the critical frequency determined by the length of the traces.
2. If a guard trace is used, it should be connected at least at both ends to ground. For frequencies above the critical frequency, guard traces should not be used to avoid resonances. Rather, user a wider separation between the traces (e.g. as if the guard trace had been there: three trace widths).
3. A greater separation distance between traces reduces crosstalk. But this is effective only if the traces are routed over a wide ground plane. If the ground return is only a thin trace, separating the signal lines will actually increase the loop areas of these lines and hence the mutual induction.
4. If ground planes are used under traces to help reduce crosstalk, make sure they have no apertures!
5. Check that all traces have a corresponding return conductor (plane rather) nearby. If “forgotten”, the return current will find a path “naturally”, usually leading to large ground loops. These large loops are not only detrimental to “signal integrity” but also to crosstalk through mutual induction between such loops!

Chapter 7

Inductance of Capacitor: Vias and Value

Contents

7.1 Demonstrations on the Inductance of Capacitor: Vias and Value Board

The Inductance of Capacitor: Vias and Value Board demonstrates the effects of parasitic inductance either caused by layout “errors” or as a result of component-internal conductor geometries. The latter usually increase with component size/value.

7.2 Inductance of Capacitor: Vias and Value Board Views

7.2.1 The Finished Board

The end result of the assembly of the Inductance of Capacitor: Vias and Value Board is shown in Figure 7.1

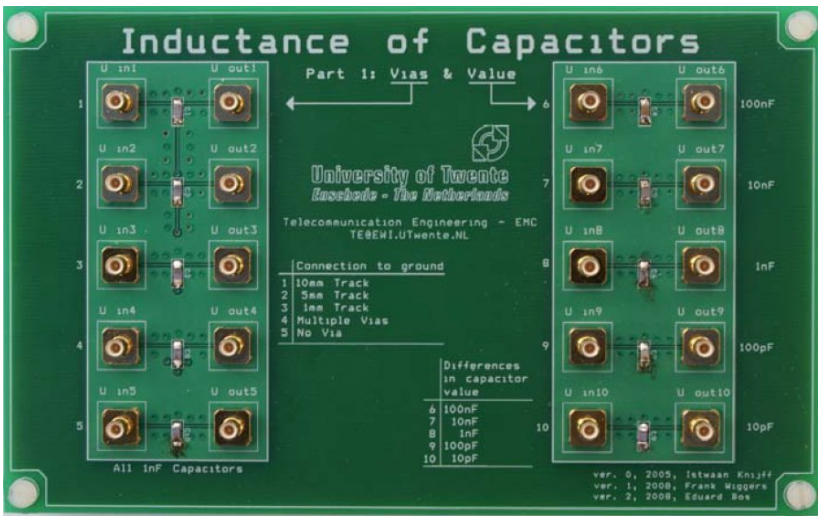

Figure 7.1: The Finished Inductance of Capacitor: Vias and Value Board.

7.2.2 The Silkscreen

The Silkscreen of the Inductance of Capacitor: Vias and Value Board shows where which components should be mounted:

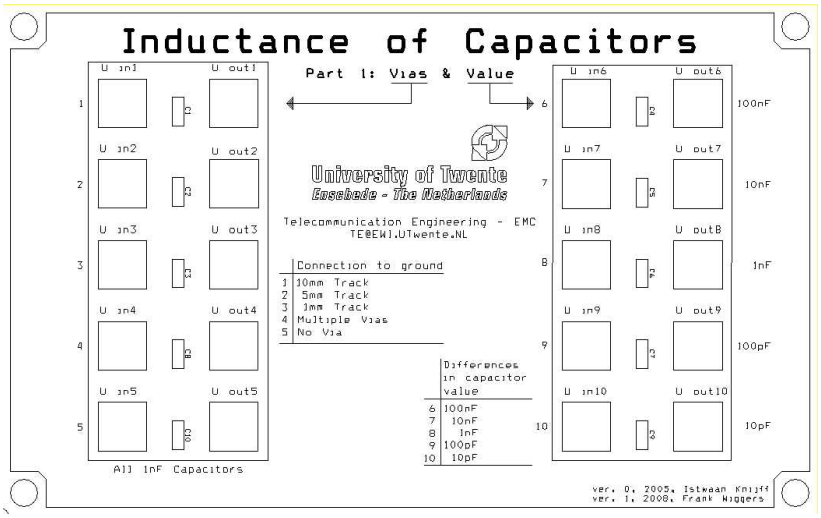

Figure 7.2: The Inductance of Capacitor: Vias and Value Board Silk Screen.

7.2.3 Bare Board Top View

The etch pattern of the empty board, seen from the top side, is shown in Figure 7.3.

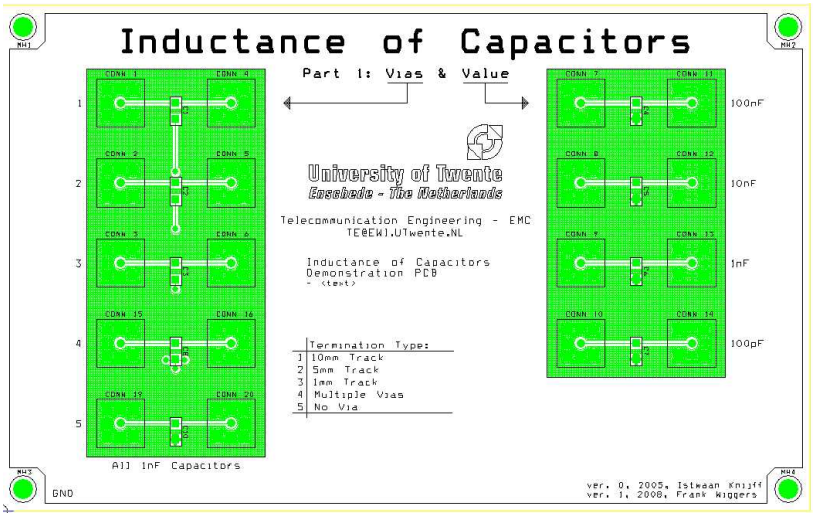

Figure 7.3: The Inductance of Capacitor: Vias and Value Bare Board (Top View)

7.2.4 Bare Board Bottom View

The etch pattern of the empty board, seen from the bottom side, is shown in Figure 7.4.

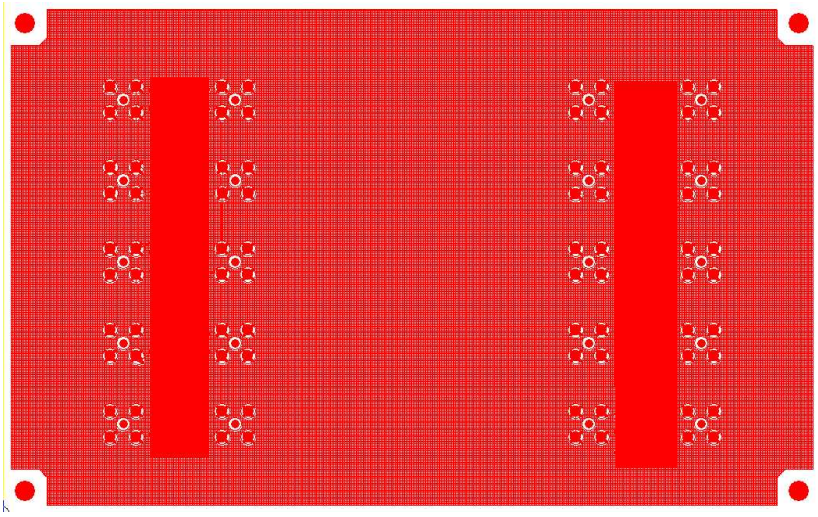

Figure 7.4: The Inductance of Capacitor: Vias and Value Bare Board (Bottom View)

7.2.5 The Board Schematic

The schematic diagram of the Inductance of Capacitor: Vias and Value Board is shown in Figure 7.5

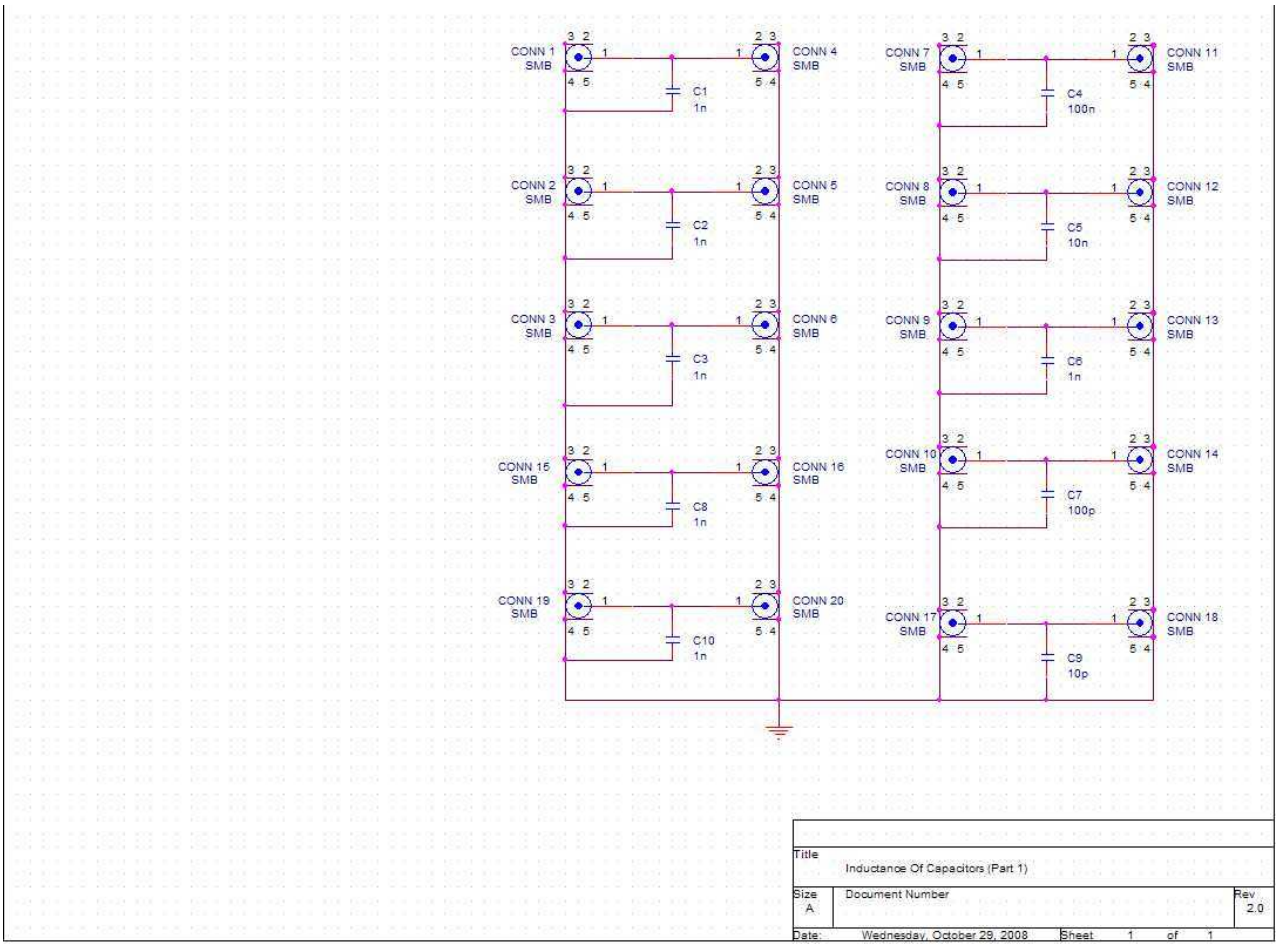

Figure 7.5: The Inductance of Capacitor: Vias and Value Board Schematic.

7.2.6 The Bill of Materials

The components to complete the Inductance of Capacitor: Vias and Value Board are shown in Table 7.1.

Table 7.1: Bill of Materials of the Inductance of Capacitor: Vias and Value Board

REF DES	VALUE	PACKAGE	FOOTPRINT
C1	1n	C	SM/C_1206
C2	1n	C	SM/C_1206
C3	1n	C	SM/C_1206

Table 7.1: Bill of Materials of the Inductance of Capacitor: Vias and Value Board (cont'd)

REF DES	VALUE	PACKAGE	FOOTPRINT
C4	100n	C	SM/C_1206
C5	10n	C	SM/C_1206
C6	1n	C	SM/C_1206
C7	100p	C	SM/C_1206
C8	1n	C	SM/C_1206
C10	1n	C	SM/C_1206
CONN 1	SMB	SMB	RF/SMB/V
CONN 2	SMB	SMB	RF/SMB/V
CONN 3	SMB	SMB	RF/SMB/V
CONN 4	SMB	SMB	RF/SMB/V
CONN 5	SMB	SMB	RF/SMB/V
CONN 6	SMB	SMB	RF/SMB/V
CONN 7	SMB	SMB	RF/SMB/V
CONN 8	SMB	SMB	RF/SMB/V
CONN 9	SMB	SMB	RF/SMB/V
CONN 10	SMB	SMB	RF/SMB/V
CONN 11	SMB	SMB	RF/SMB/V
CONN 12	SMB	SMB	RF/SMB/V
CONN 13	SMB	SMB	RF/SMB/V
CONN 14	SMB	SMB	RF/SMB/V
CONN 15	SMB	SMB	RF/SMB/V
CONN 16	SMB	SMB	RF/SMB/V
CONN 19	SMB	SMB	RF/SMB/V
CONN 20	SMB	SMB	RF/SMB/V

7.3 Board Functional Description

The "Inductance of Capacitor Vias and Value" Board is the first (part 1) of a three part set. It addresses the parasitic effects which are caused partly by the way the capacitors are built and partly by the placement and routing on the board. Apart from the capacitance for which these devices are sold, they come with an Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL). This inductance will resonate with the capacitance at a frequency determined by the actual value of capacitance and inductance. This is a series resonance which has the characteristic frequency response shown in Figure 7.6. The lowest point in the graph indicates the value of the "Equivalent Series Resistor" (ESR).

It is clear from Figure 7.6 that the capacitor no longer performs as a capacitor for frequencies over $f_{resonance}$.

The Inductance of Capacitor: Vias and Value Board focusses on the layout of the Board and on the effect of capacitance values. The effects are best viewed in the frequency domain. On the left hand side of the board, it has a number of identical 1 nF capacitors which are connected to the

return ground plane with traces decreasing in length from the top of the board to the bottom. This can be seen in figures 7.1 and 7.3. On the right hand side capacitors with identical shape but with decreasing value are mounted (without additional trace lengths). As done in earlier experiments, a spectrum analyzer with tracking generator with two test cables is calibrated to show 0 dB over the frequency range of interest when the cables are directly interconnected. We used 1 GHz as highest frequency. The the cables are connected at either end of the capacitor to measure its effectiveness as decoupling capacitor. The results for the left hand row of (identical) capacitors is shown in Figure 7.7. The results of measurements on the right hand side capacitors with identical shape but decreasing value is shown in Figure 7.8

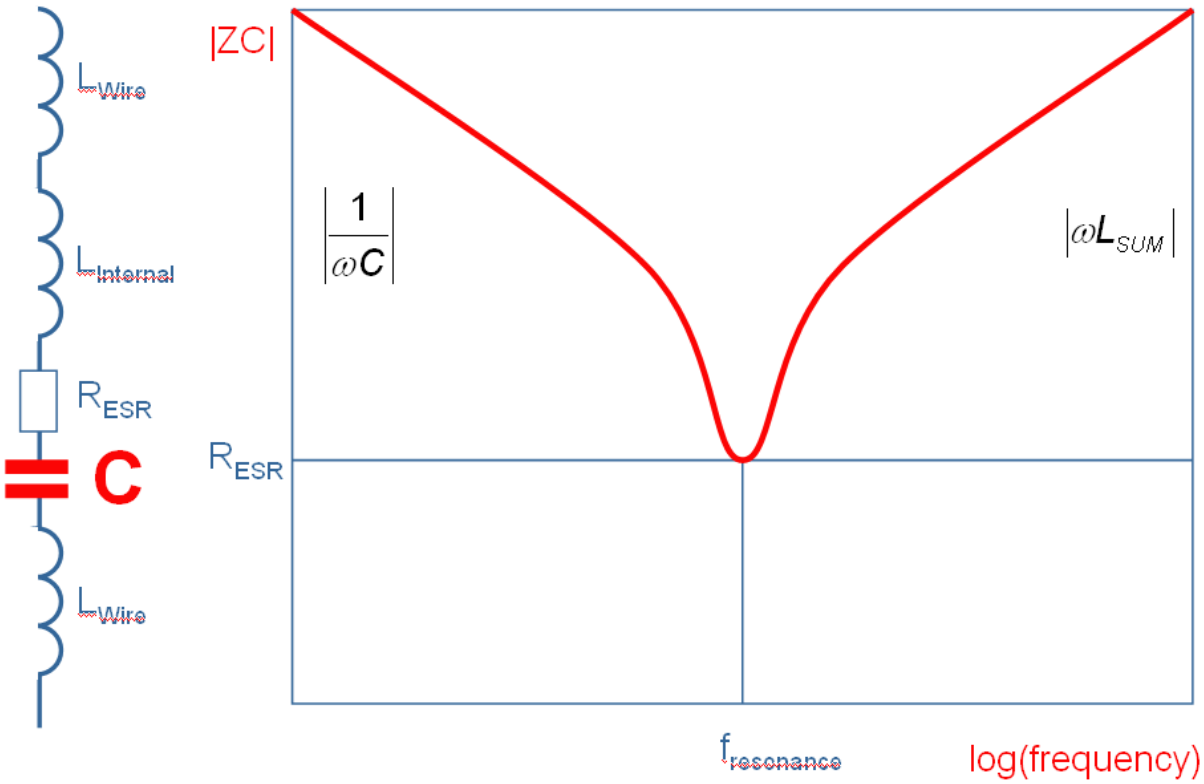

Figure 7.6: Typical Frequency Response of a Decoupling Capacitor

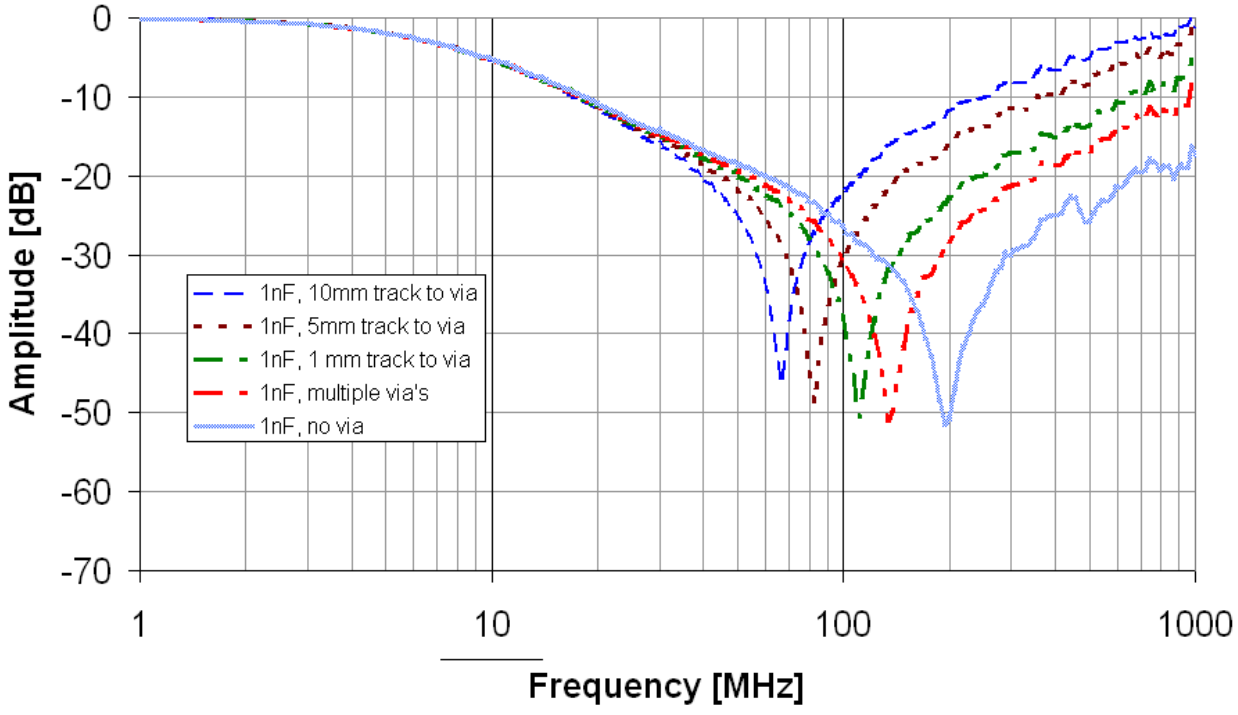

Figure 7.7: Frequency Response of Identical Capacitors with Additional Trace Lengths

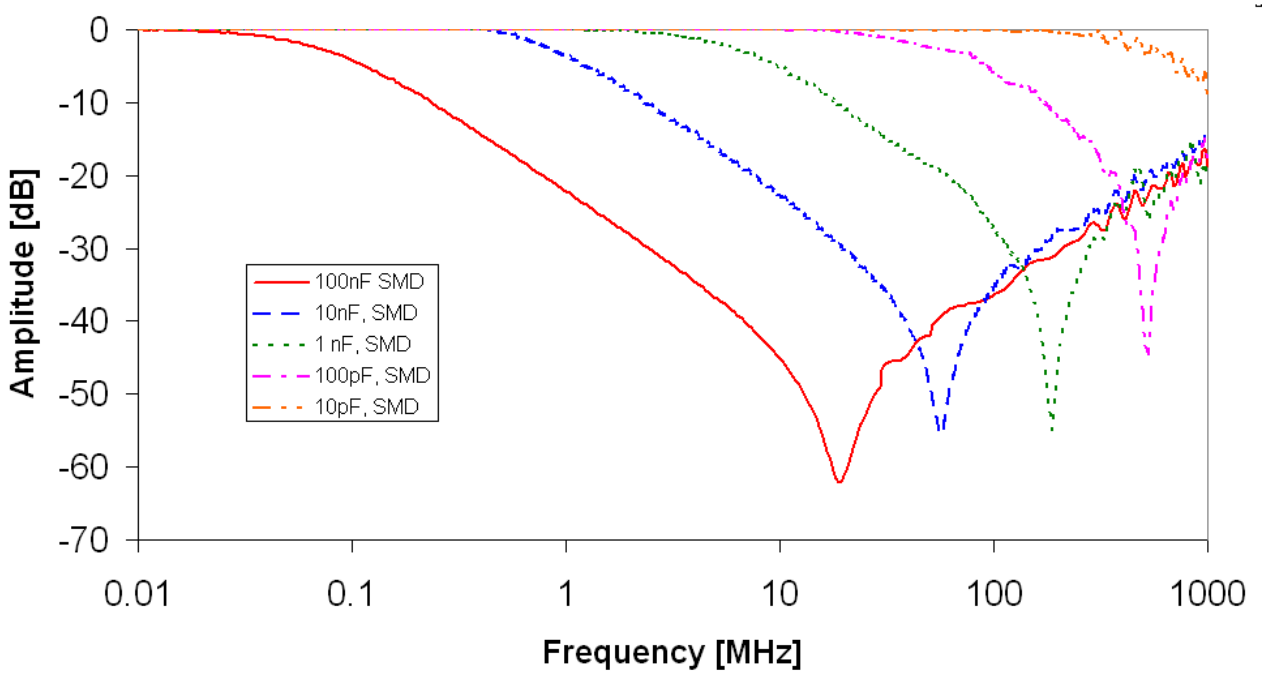

Figure 7.8: Frequency Response of Capacitors with Decreasing Values

7.4 Lessons Learned

The “Inductance of Capacitor: Vias and Value Board” experiments show that:

1. Increasing the length of a connecting trace increases the amount of parasitic inductance of a decoupling capacitor. This lowers its inherent resonance frequency and hence, the useable frequency range for decoupling purposes.
2. A higher value capacitor tends to have a higher parasitic inductance. The effect, again, is resonance at a lower frequency and a lower useable frequency range for decoupling.

Chapter 8

Inductance of Capacitor: Dielectrics

Contents

8.1 Demonstrations on the Inductance of Capacitor: Dielectrics Board

The Inductance of Capacitor, Dielectrics Board shows the effect of the dielectric material of a (decoupling) capacitor on its parasitic properties Equivalent Series Inductance (ESI) and Equivalent Series Resistance (ESR).

8.2 Inductance of Capacitor: Dielectrics Board Views

8.2.1 The Finished Board

The end result of the assembly of the Inductance of Capacitor: Dielectrics Board is shown in Figure 8.1

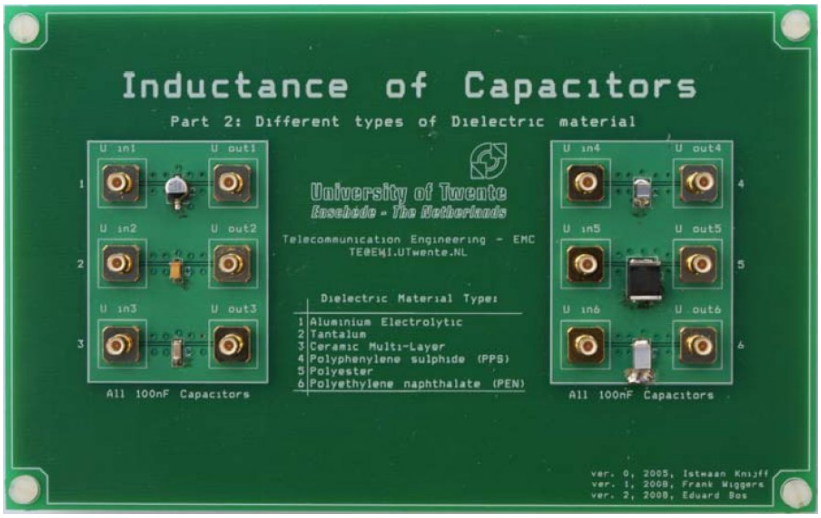

Figure 8.1: The Finished Inductance of Capacitor: Dielectrics Board.

8.2.2 The Silkscreen

The Silkscreen of the Inductance of Capacitor: Dielectrics Board shows where which components should be mounted:

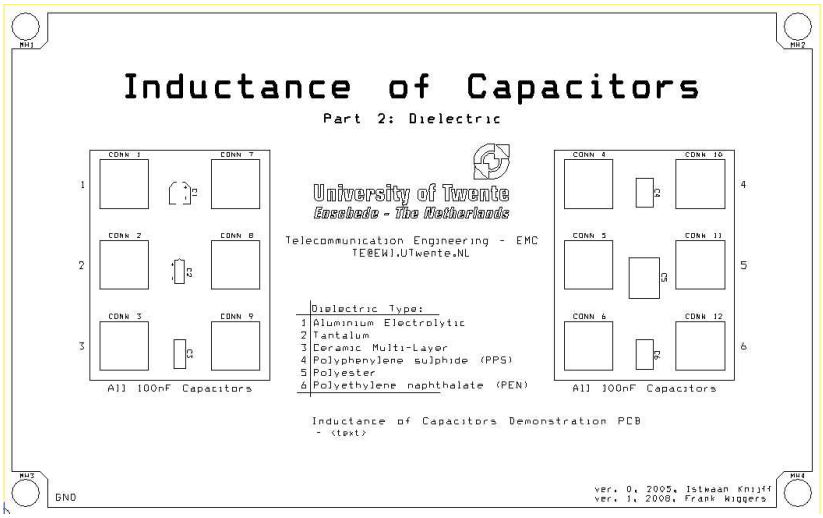

Figure 8.2: The Inductance of Capacitor: Dielectrics Board Silk Screen.

8.2.3 Bare Board Top View

The etch pattern of the empty board, seen from the top side, is shown in Figure 8.3.

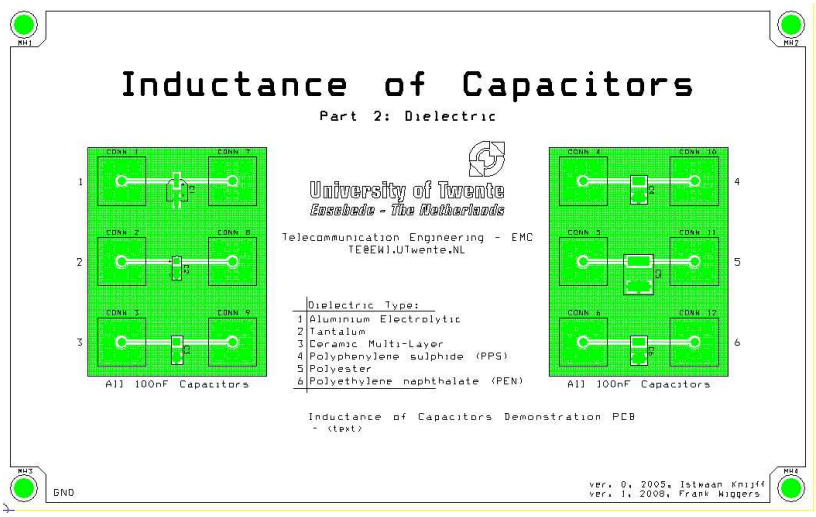

Figure 8.3: The Inductance of Capacitor: Dielectrics Bare Board (Top View)

8.2.4 Bare Board Bottom View

The etch pattern of the empty board, seen from the bottom side, is shown in Figure 8.4.

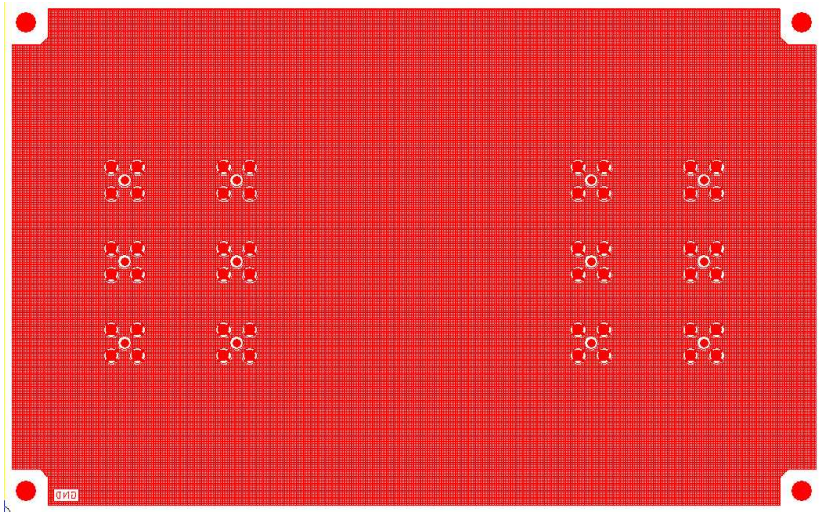

Figure 8.4: The Inductance of Capacitor: Dielectrics Bare Board (Bottom View)

8.2.5 The Board Schematic

The schematic diagram of the Inductance of Capacitor: Dielectrics Board is shown in Figure 8.5

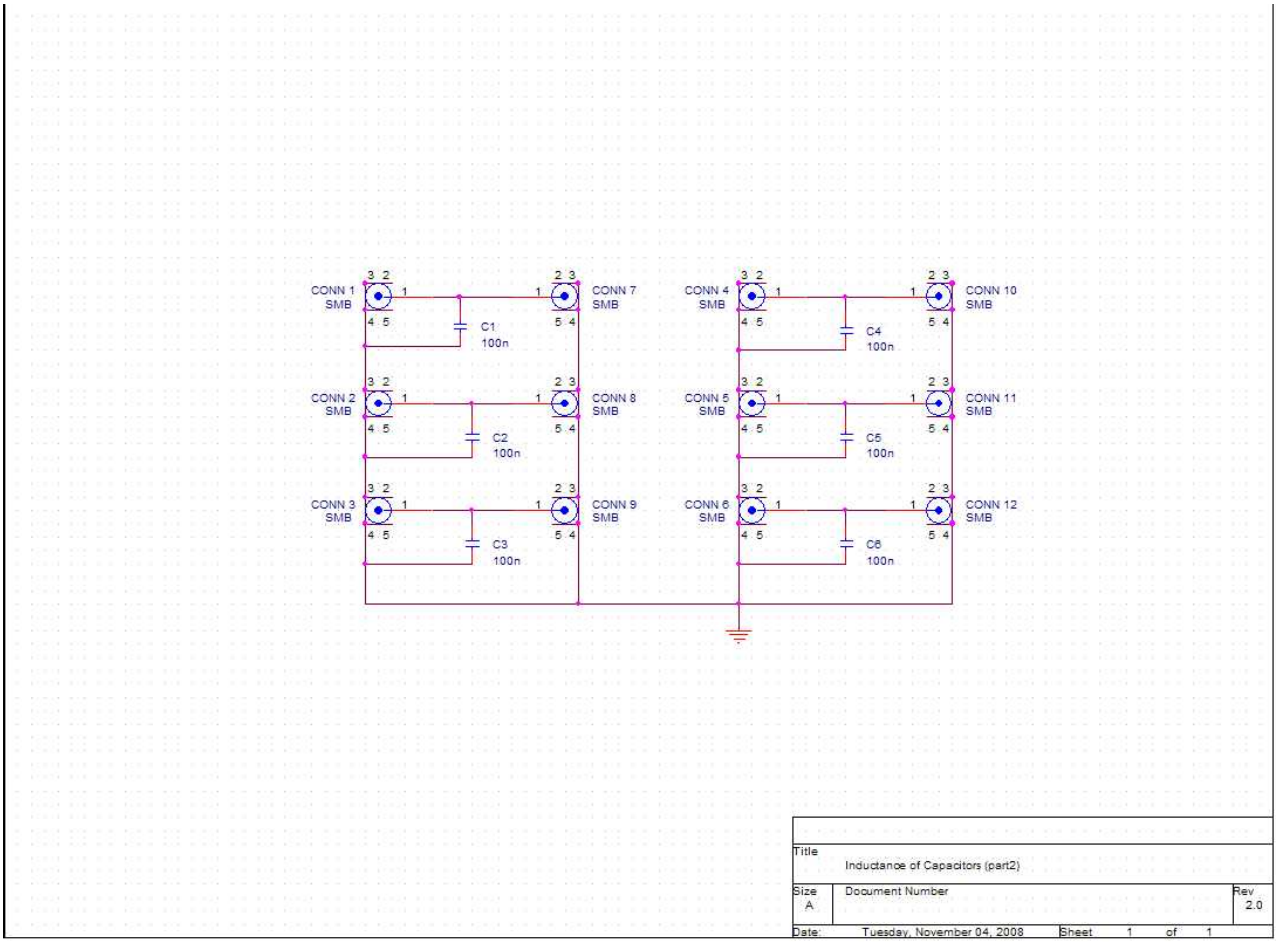

Figure 8.5: The Inductance of Capacitor: Dielectrics Board Schematic.

8.2.6 The Bill of Materials

The components to complete the Inductance of Capacitor: Dielectrics Board are shown in Table 8.1.

Table 8.1: Bill of Materials of the Inductance of Capacitor: Dielectrics Board

REF DES	VALUE	PACKAGE	FOOTPRINT
C1	100n	C	SMD.ELCO.4MM
C2	100n	C	SMD.TANTALUM.CASE_A
C3	100n	C	SM/C_1206
C4	100n	C	SM/C_1210

Table 8.1: Bill of Materials of the Inductance of Capacitor: Dielectrics Board (cont'd)

REF DES	VALUE	PACKAGE	FOOTPRINT
C5	100n	C	SM/L_2220
C6	100n	C	SM/C_1210
CONN 1	SMB	SMB	RF/SMB/V
CONN 2	SMB	SMB	RF/SMB/V
CONN 3	SMB	SMB	RF/SMB/V
CONN 4	SMB	SMB	RF/SMB/V
CONN 5	SMB	SMB	RF/SMB/V
CONN 6	SMB	SMB	RF/SMB/V
CONN 7	SMB	SMB	RF/SMB/V
CONN 8	SMB	SMB	RF/SMB/V
CONN 9	SMB	SMB	RF/SMB/V
CONN 10	SMB	SMB	RF/SMB/V
CONN 11	SMB	SMB	RF/SMB/V
CONN 12	SMB	SMB	RF/SMB/V

8.3 Board Functional Description

The "Inductance of Capacitor: Dielectrics" Board is the second (part 2) of a 3 part set. Its operation is best viewed in the frequency domain. As its predecessor described in chapter 7 starting on page 55, it addresses the parasitic elements, largely inductance, inside a capacitor. For that purpose it has 6 capacitors of identical value (100 nF), but built with different dielectric materials. It is operated as the board of chapter 7, described in Section 7.3 on page 59. The results of the measurements are shown in Figure 8.6. Figure 8.6 shows that both the resonant frequency and the equivalent series resistance are affected by the way a capacitor is built.

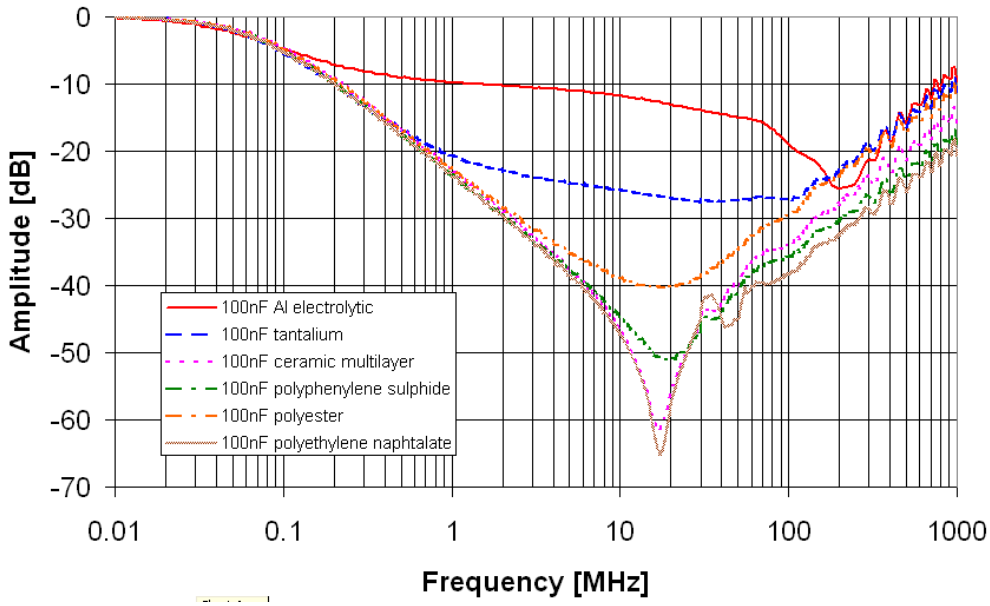

Figure 8.6: The effect of different dielectrics in 6 100 nF capacitors

8.4 Lessons Learned

The “Inductance of Capacitor: Dielectrics” experiments show that:

1. The way a capacitor is built has an effect on its parasitic inductance. The resonance frequency and inherent useable frequency range are affected by it.
2. The way a capacitor is built has an effect on its equivalent series resistance. The minimum value the decoupling capacitor impedance can reach is determined by it.

Chapter 9

Inductance of Capacitor: Packaging

Contents

9.1 Demo's with the Inductance of Capacitor: Packaging Board

Capacitors come in different shapes and sizes. The packaging affects the device parasitic elements and hence its behavior over frequency.

9.2 Inductance of Capacitor: Packaging Board Views

9.2.1 The Finished Board

The end result of the assembly of the Inductance of Capacitor: Packaging Board is shown in Figure 9.1

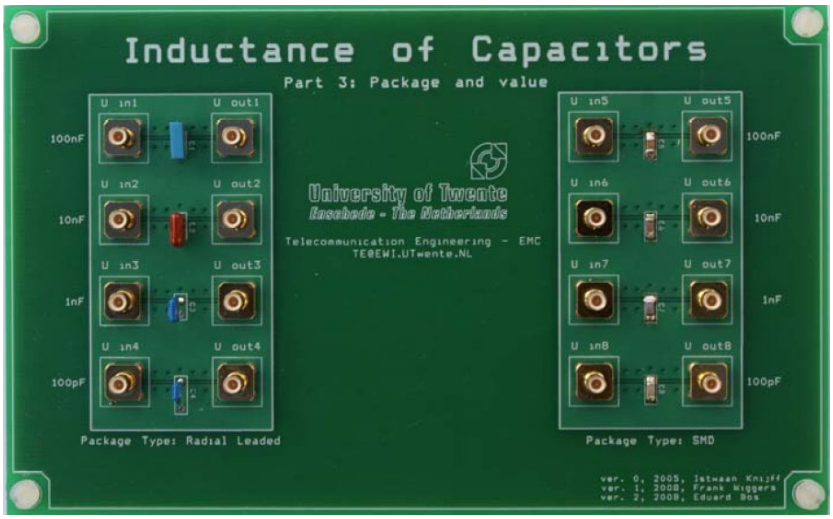

Figure 9.1: The Finished Inductance of Capacitor: Packaging Board.

9.2.2 The Silkscreen

The Silkscreen of the Inductance of Capacitor: Packaging Board shows where which components should be mounted:

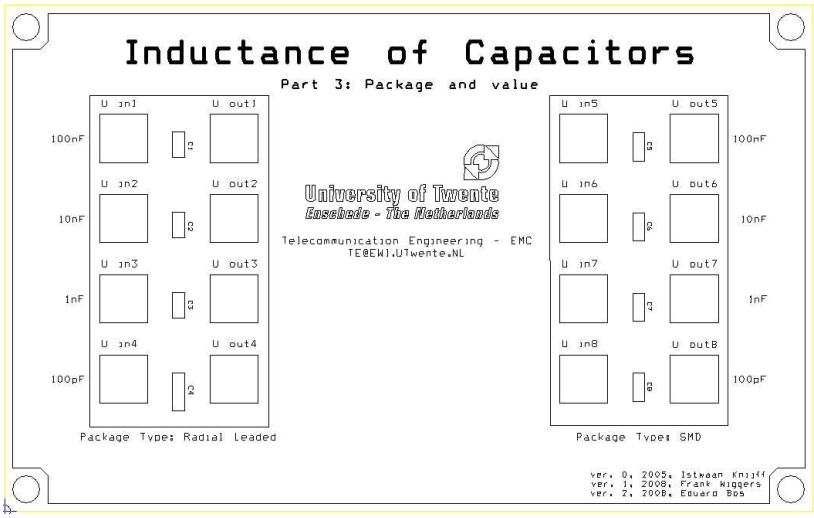

Figure 9.2: The Inductance of Capacitor: Packaging Board Silk Screen.

9.2.3 Bare Board Top View

The etch pattern of the empty board, seen from the top side, is shown in Figure 9.3.

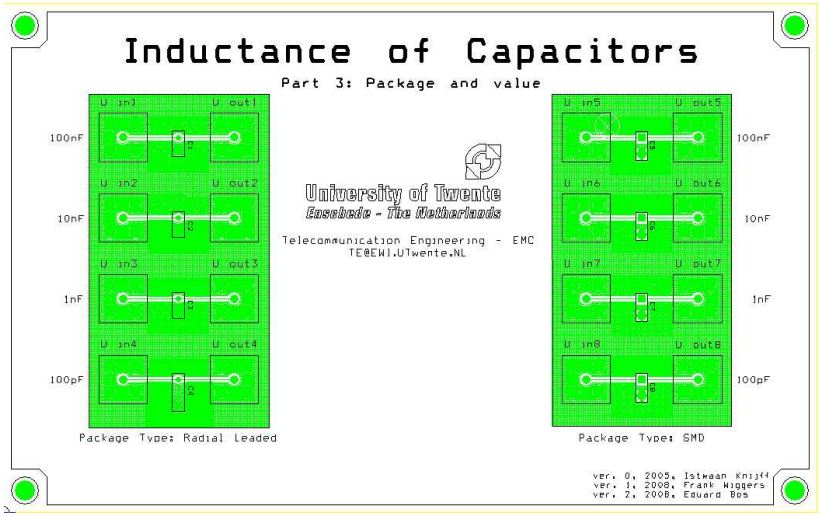

Figure 9.3: The Inductance of Capacitor: Packaging Bare Board (Top View)

9.2.4 Bare Board Bottom View

The etch pattern of the empty board, seen from the bottom side, is shown in Figure 9.4.

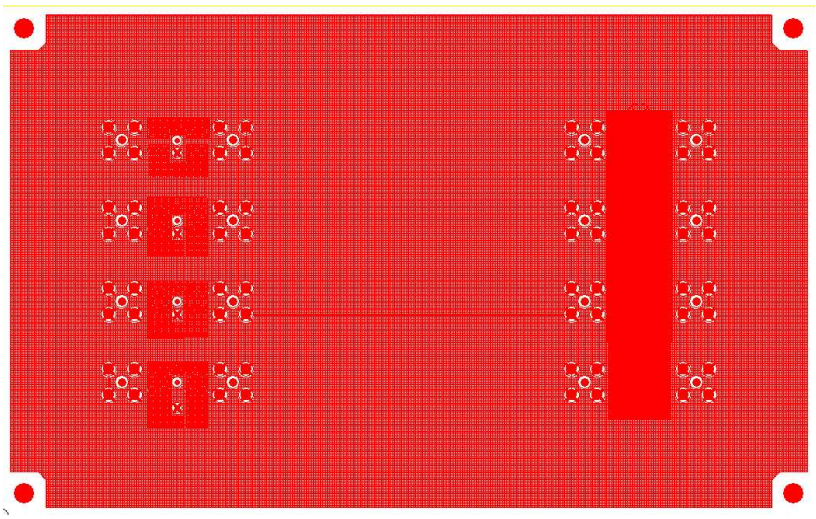

Figure 9.4: The Inductance of Capacitor: Packaging Bare Board (Bottom View)

9.2.5 The Board Schematic

The schematic diagram of the Inductance of Capacitor: Packaging Board is shown in Figure 9.5

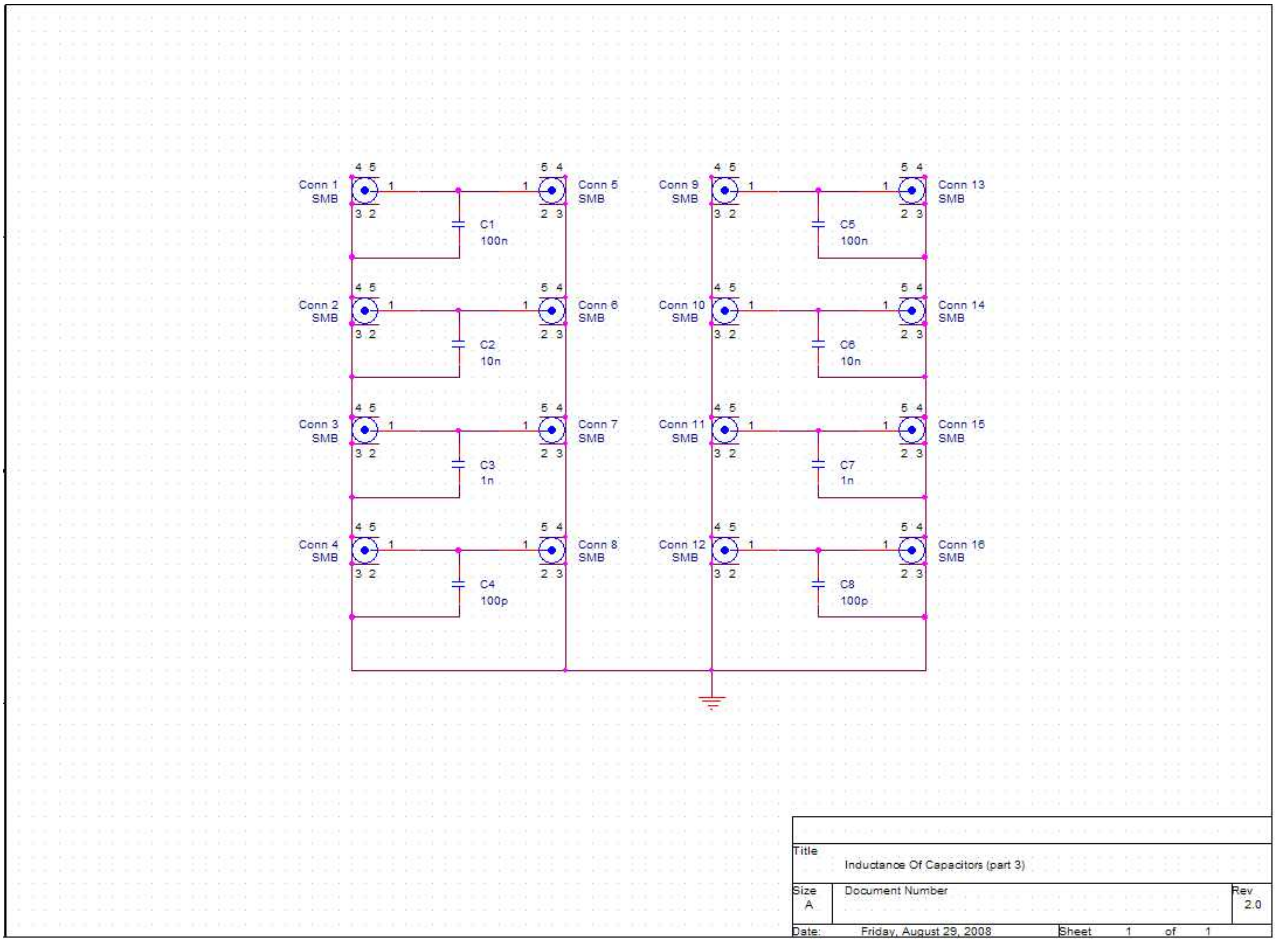

Figure 9.5: The Inductance of Capacitor: Packaging Board Schematic.

9.2.6 The Bill of Materials

The components to complete the Inductance of Capacitor: Packaging Board are shown in Table 9.1.

Table 9.1: Bill of Materials of the Inductance of Capacitor: Packaging Board

REF DES	VALUE	PACKAGE	FOOTPRINT
C1	100n	C	LEADED.CERAMIC.C315
C2	10n	C	LEADED.CERAMIC.C315
C3	1n	C	LEADED.CERAMIC.C315
C4	100p	C	LEADED.CERAMIC.C317
C5	100n	C	SM/C_1206
C6	10n	C	SM/C_1206
C7	1n	C	SM/C_1206
C8	100p	C	SM/C_1206
CONN 1	SMB	SMB	RF/SMB/V
CONN 2	SMB	SMB	RF/SMB/V
CONN 3	SMB	SMB	RF/SMB/V
CONN 4	SMB	SMB	RF/SMB/V
CONN 5	SMB	SMB	RF/SMB/V
CONN 6	SMB	SMB	RF/SMB/V
CONN 7	SMB	SMB	RF/SMB/V
CONN 8	SMB	SMB	RF/SMB/V
CONN 9	SMB	SMB	RF/SMB/V
CONN 10	SMB	SMB	RF/SMB/V
CONN 11	SMB	SMB	RF/SMB/V
CONN 12	SMB	SMB	RF/SMB/V
CONN 13	SMB	SMB	RF/SMB/V
CONN 14	SMB	SMB	RF/SMB/V
CONN 15	SMB	SMB	RF/SMB/V
CONN 16	SMB	SMB	RF/SMB/V

9.3 Board Functional Description

The “Inductance of Capacitor: Packaging” Board is the third (part 3) of a 3 part set. Its operation is best viewed in the frequency domain. It is focussed on parasitic effects in capacitors, as its predecessors. The board is operated as the board of chapter 7, described in Section 7.3 on page 59. The board has two rows of capacitors with decreasing values from 100 nF, 10 nF, 1 nF to 100 pF. The left hand row has leaded components while the right hand side features SMD versions. The results of the measurements are shown per capacitor value for comparison in Figure 9.6 for the 100 nF, Figure 9.7 for the 10 nF, Figure 9.8 for the 1 nF and Figure 9.9 for the 100 pF capacitors.

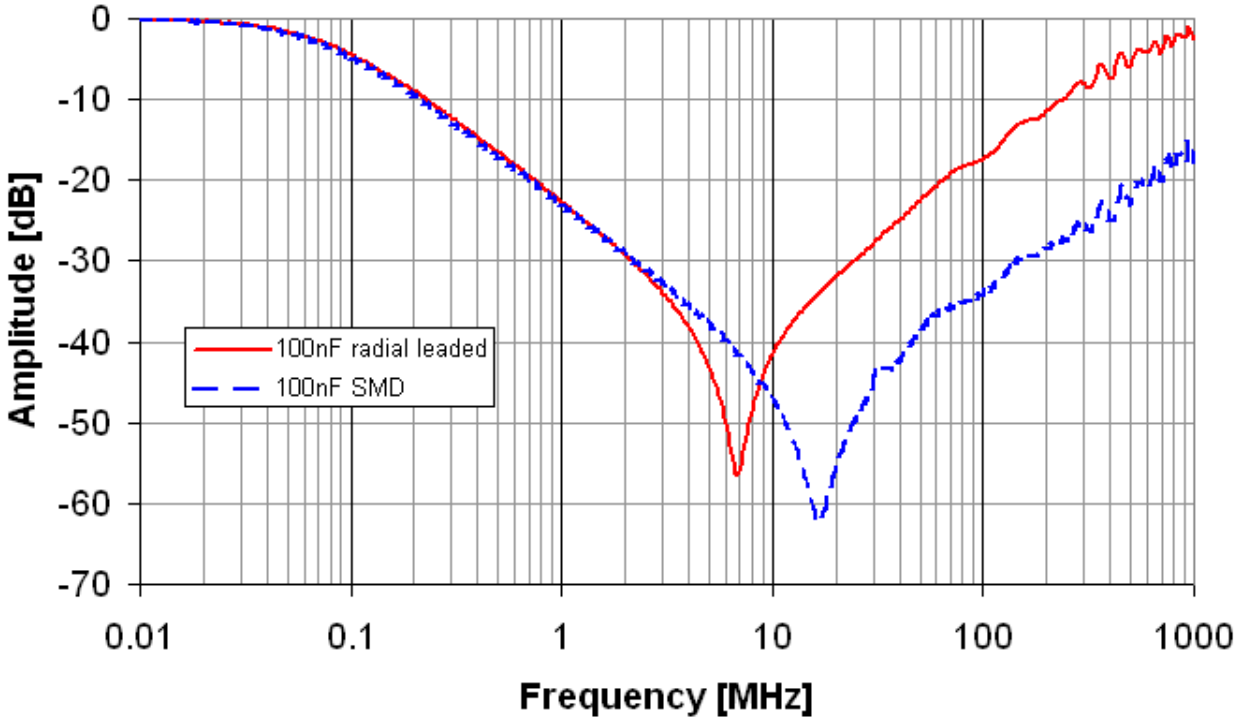

Figure 9.6: Inductance of Capacitor: Packaging Board Responses of the two 100 nF versions

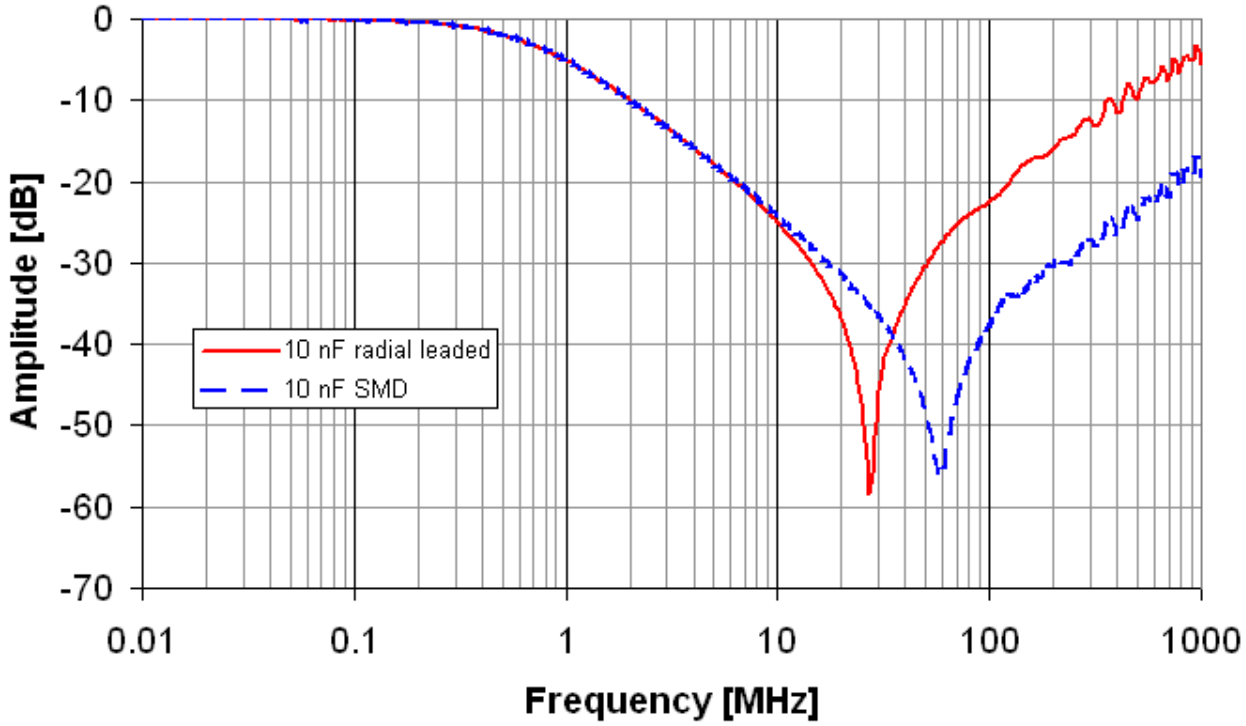

Figure 9.7: Inductance of Capacitor: Packaging Board Responses of the two 10 nF versions

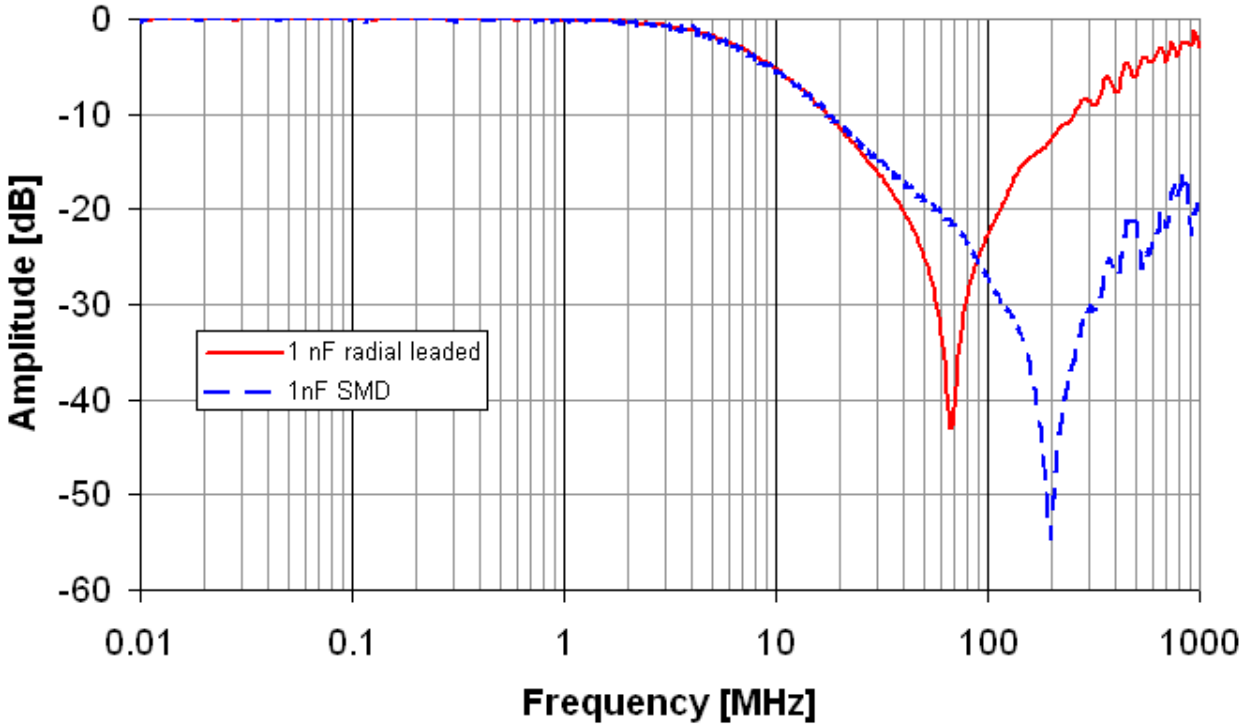

Figure 9.8: Inductance of Capacitor: Packaging Board Responses of the two 1 nF versions

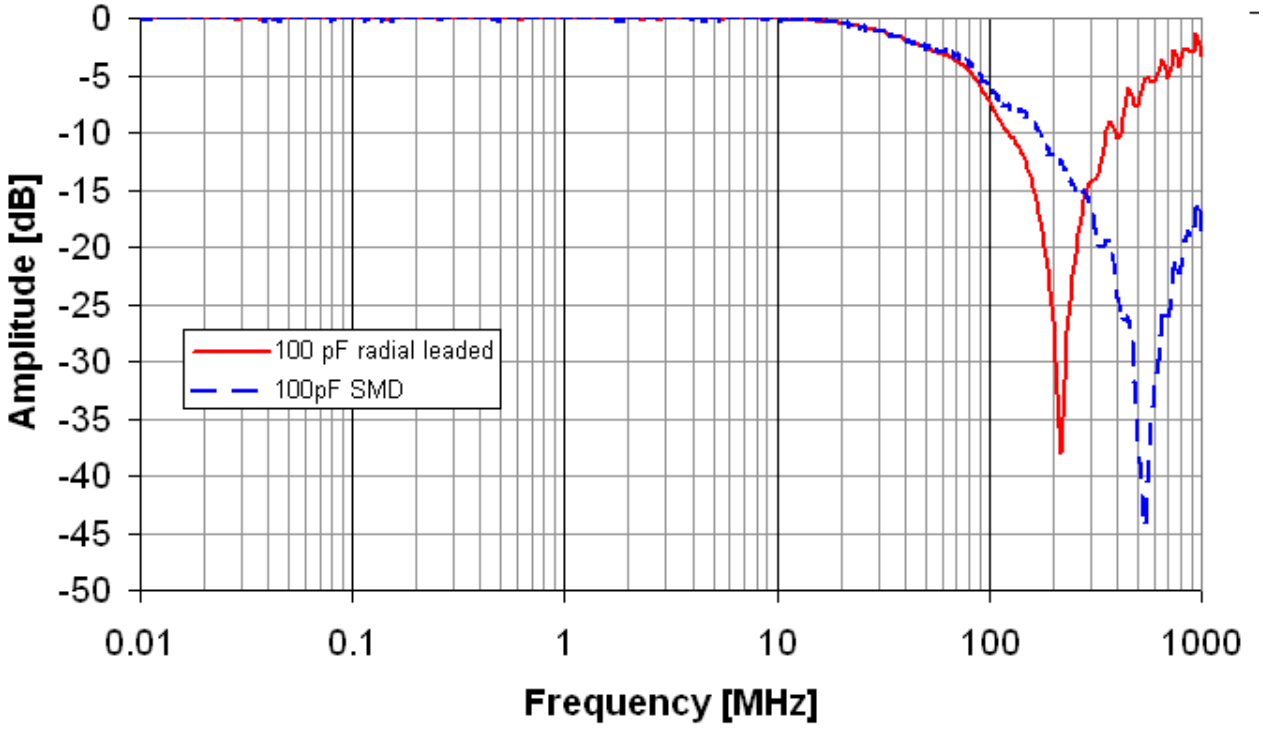

Figure 9.9: Inductance of Capacitor: Packaging Board Responses of the two 100 pF versions

9.4 Lessons Learned

The “Inductance of Capacitor: Packaging” experiments show that:

- The packaging of the capacitor has an influence on the parasitic inductance and resistance of the device. This influences the useable frequency range for decoupling.

Chapter 10

Grounding of Filters

Contents

10.1 Demonstrations on the Grounding of Filters Board

The Grounding of Filters Board demonstrates the effect of the way filters are mounted. It shows that induction in the ground return path seriously impairs the filter's effectiveness.

10.2 Grounding of Filters Board Views

10.2.1 The Finished Board

The end result of the assembly of the Grounding of Filters is shown in Figure 10.1

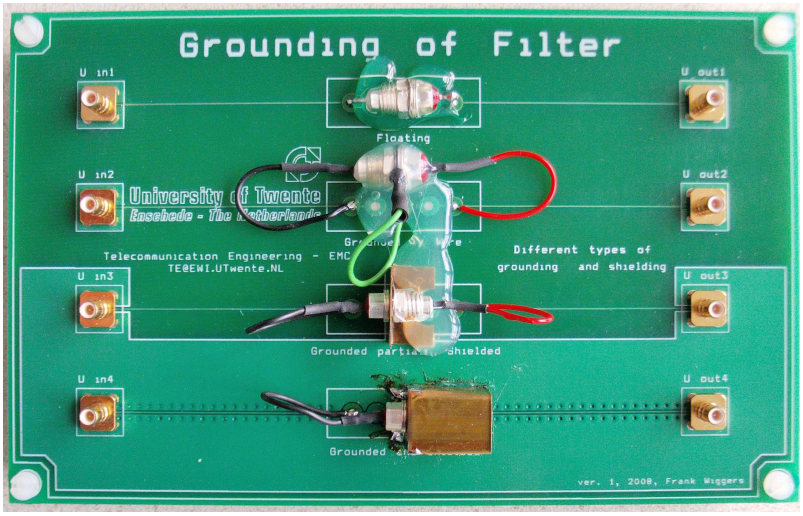

Figure 10.1: The Finished Grounding of Filters Board.

10.2.2 The Silkscreen

The Silkscreen of the Grounding of Filters Board shows where which components should be mounted:

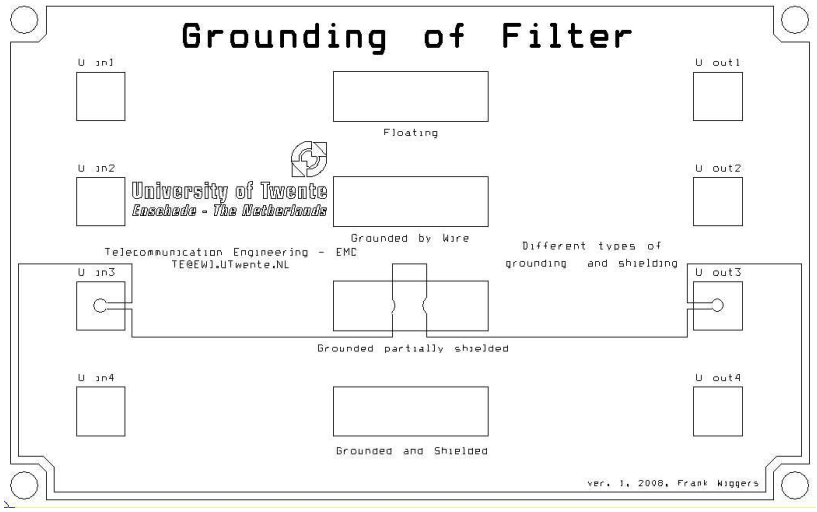

Figure 10.2: The Grounding of Filters Board Silk Screen.

10.2.3 Bare Board Top View

The etch pattern of the empty board, seen from the top side, is shown in Figure 10.3.

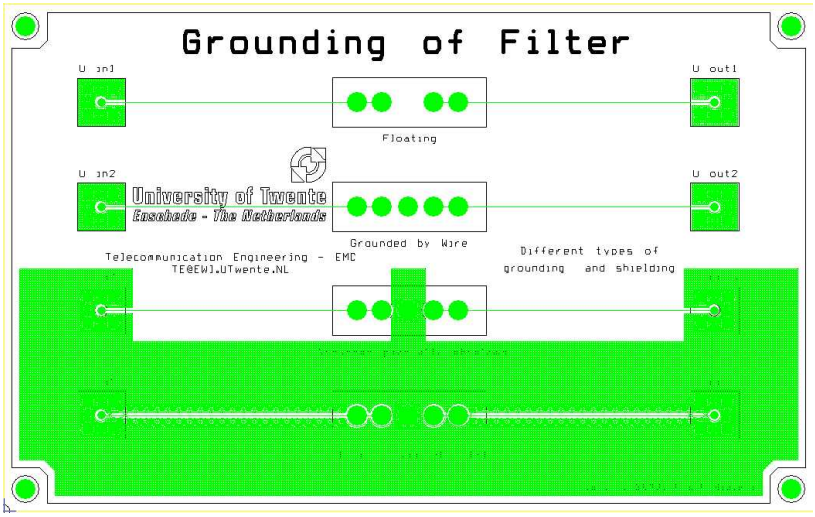

Figure 10.3: The Grounding of Filters Bare Board (Top View)

10.2.4 Bare Board Bottom View

The etch pattern of the empty board, seen from the bottom side, is shown in Figure 10.4.

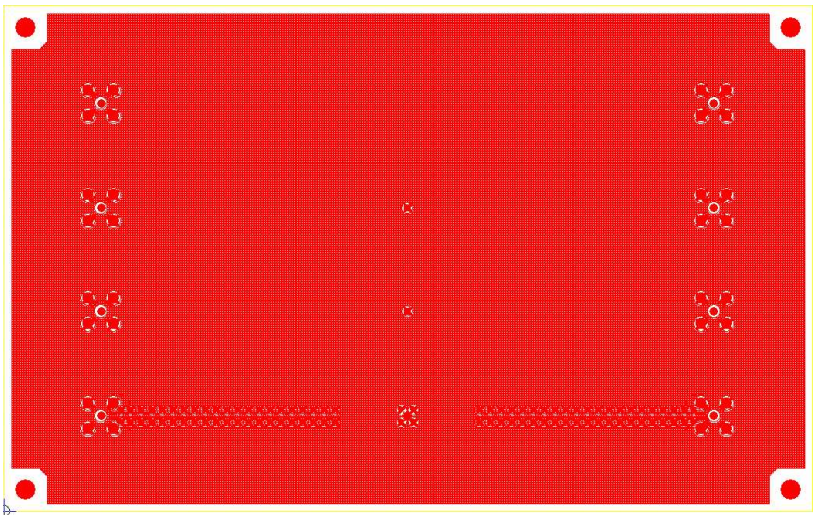

Figure 10.4: The Grounding of Filters Bare Board (Bottom View)

10.2.5 The Board Schematic

The schematic diagram of the Grounding of Filters Board is shown in Figure 10.5

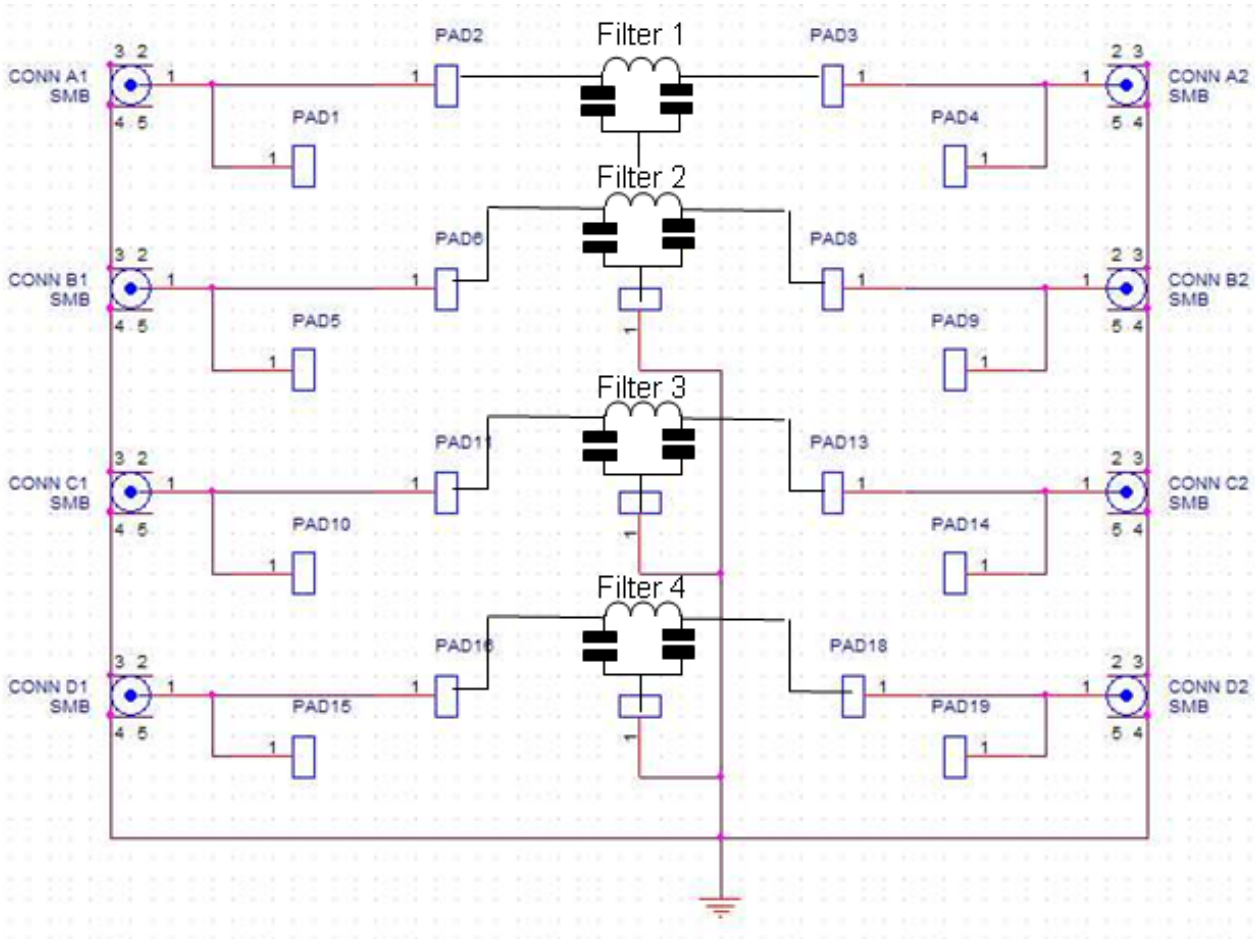

Figure 10.5: The Grounding of Filters Board Schematic.

10.2.6 The Bill of Materials

The components to complete the Grounding of Filters Board are shown in Table 10.1.

Table 10.1: Bill of Materials of the Grounding of Filters Board

REF DES	VALUE	PACKAGE	FOOTPRINT
U in1	SMB	SMB	RF/SMB/V
U in2	SMB	SMB	RF/SMB/V
U in3	SMB	SMB	RF/SMB/V
U in4	SMB	SMB	RF/SMB/V
U out1	SMB	SMB	RF/SMB/V
U out2	SMB	SMB	RF/SMB/V

Table 10.1: Bill of Materials of the Grounding of Filters Board (cont'd)

REF DES	VALUE	PACKAGE	FOOTPRINT
U out3	SMB	SMB	RF/SMB/V
U out4	SMB	SMB	RF/SMB/V
Filter 1 - 4	Low Pass(PI), several MHz	feedthrough	(e.g. Oxley FLTM/P/1500; Farnell 1570100)
Wire	AWG 24	40 cm	Flexible type
Metal Bracket	5x12mm	L-shape	Home made
Copper tape	5cm	12mm wide	3M

10.3 Board Functional Description

The Grounding of Filters Board intends to show how the way a filter is built into a system or rather, the geometry of the return path for signals the filter is supposed to stop, affects the behavior of the filter. As can be seen in Figure 10.1, the board has four identical filters, mounted in different ways. According to the manufacturers specification the attenuation of frequencies over 10 MHz should be better than 50 dB. The board has four input and four output connectors. Traces run from the connectors towards the middle of the board where the filters have been mounted. The bottom of the board has a wide ground plane under all traces. The details of the mounting of the filters are:

1. The first filter between connectors U in1 and U out1 is only touching the board with its signal in and output terminals. In other words, it has no ground connection.
2. The second filter is connected with long (about 5 cm) wires but has a ground wire too.
3. The third filter has input and output wires but is mounted to a sturdy and relatively wide metal bracket.
4. The fourth filter is mounted with the shortest possible wiring and the input section has been completely shielded by a metal enclosure. Further, this last filter section also has a ground plane on the component side of the board. The ground planes on both sides are not only connected at the connectors but also with many via's alongside the signal traces.

To fabricate the mechanical parts (for the latter two filters) 0.4 mm brass plate was used. Anything between 0.3 and 1 mm is O.K. Figure 10.6 shows the drawing of the basic shapes. These then are bent to form the bracket for the third filter (left hand side of Figure 10.6) and the enclosure for the fourth filter (right hand side of Figure 10.6). The proposed enclosure is almost shaped like a cube but two sides are missing. One open end is directed to connector "U out4". The filter output wire must be connected to the PCB "inside" the enclosure. The other open side is the bottom of the cube. It is closed by the ground plane(s) on the PCB. It is important that the bottom edge makes good contact with the top ground plane. If you are assembling the empty board, scratch of the solder resist under the edges of the enclosure and solder these edges to the PCB ground plane. This is easier if the brass material is thin! The bracket of the third filter has a small hole. A copper wire should be used to connect the bracket to the grounding hole in the PCB. The filters (the version mentioned in the bill of materials, Table 10.1) are of the symmetrical "π" type. So, the direction they

are mounted in is not important. The input wire (black in Figure 10.1) has some inductance and is needed to make the low-frequency characteristics of the filters identical. Only the fourth filter has no output wire. The connection from this filter to the board should be as short as possible. The output of this latter filter should be completely enclosed by shielding metal. The remaining open end could also be closed with e.g. copper tape. But even without this, the performance is acceptable (see Figure 10.7). This is because the remaining aperture size in the shielding enclosure is much smaller than a (half-) wavelength of the highest frequency of interest.

To see the performance of each mounting, a spectrum analyzer with tracking generator is con-

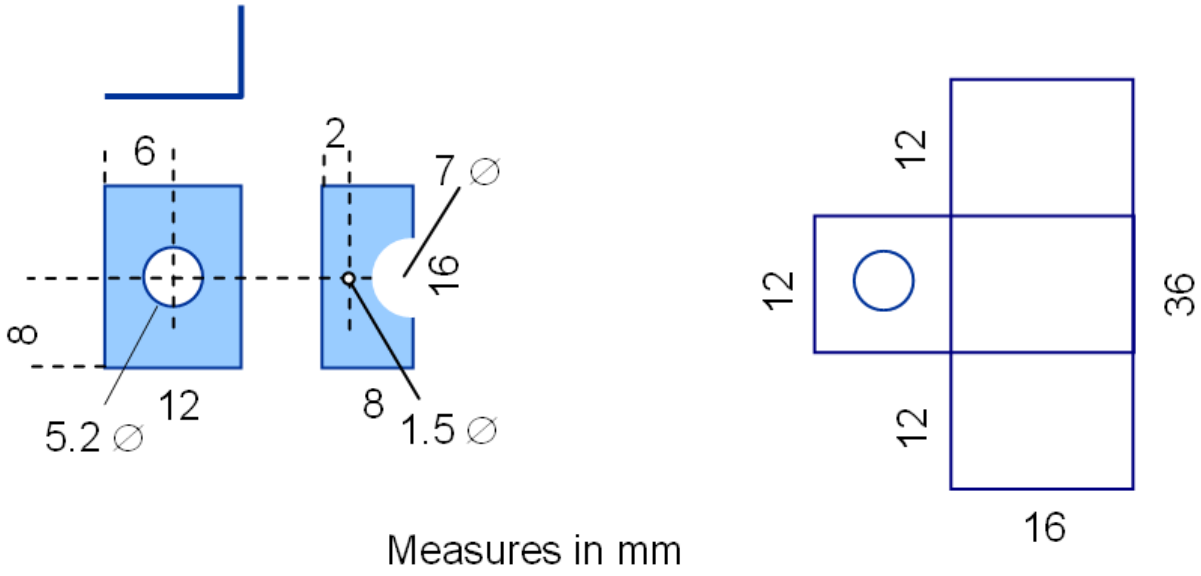

Figure 10.6: Drawing of the brass sheet material needed for filters 3 and 4

nected to measure the attenuation of each filter in sequence. The generator is connected to the U inX connector while the analyzer input is connected to the U outX connector on the board. The results are plotted together in Figure 10.7 The first, ungrounded filter does not work at all. It is characterized with the solid blue line around 0 dB. The second filter's poor performance is shown as "Filter Ground through Wire" with a green line. The third filter behaves much better. The attenuation indeed goes to -50 dB but then comes back up again. The latter effect is increased if the in and output wires are lifted from the board (and the groundplane). The fourth filter behaves as it should. Note: the situations demonstrated on this PCB are simulations of what happens with filters, mounted in a cabinet. The description for the four cases would then read:

1. A filter mounted in a plastic wall.
2. A filter mounted in a plastic wall, grounded with a long (green-yellow) wire.
3. A filter mounted inside an instrumentation cabinet (e.g. for weather protection) on a wide ground plane where in and output wiring can easily crosstalk.
4. A filter mounted in the metal wall of a shielded ("EMC") enclosure. In- and output wiring are completely separated by the shielding wall.

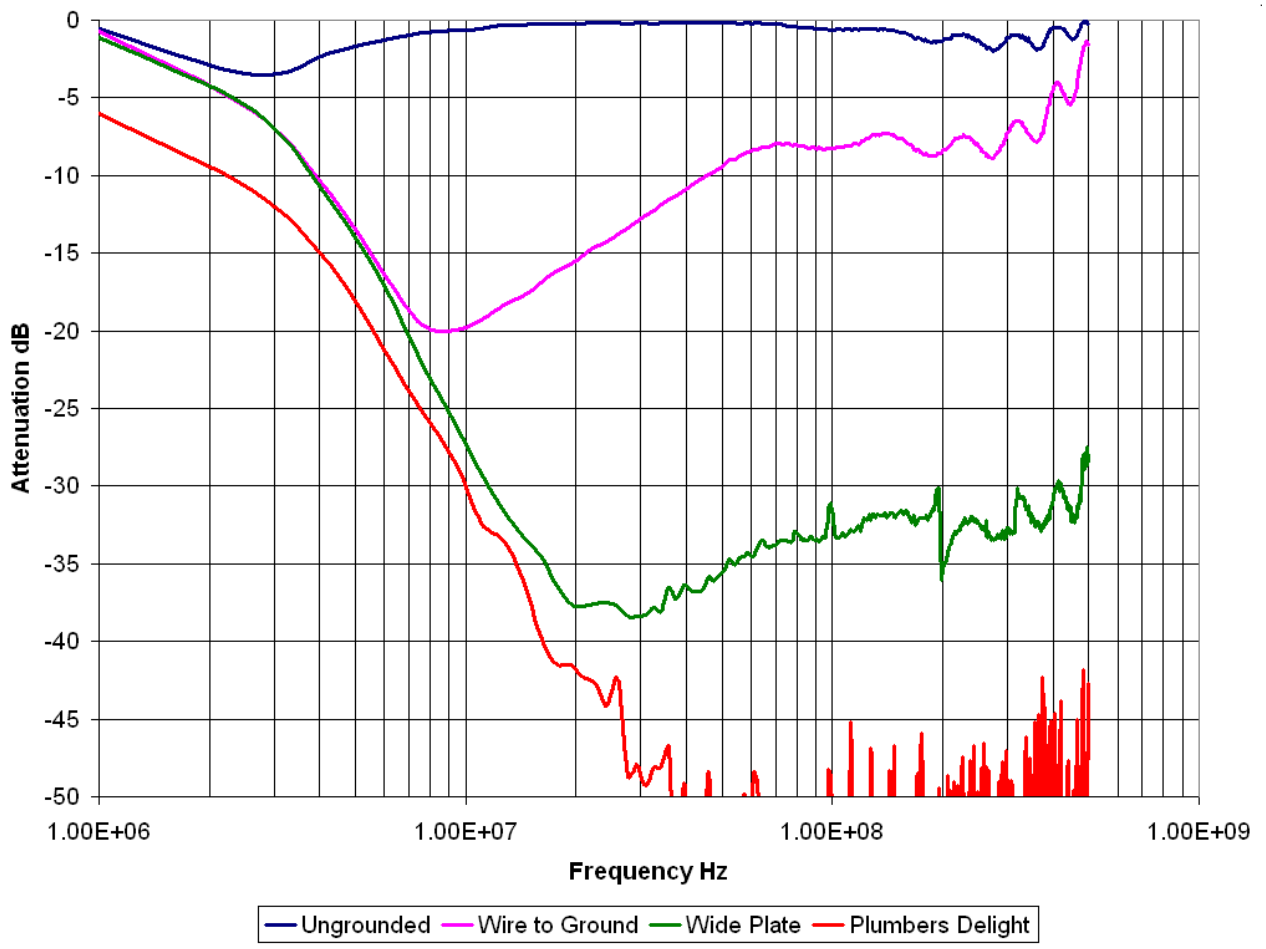

Figure 10.7: Frequency Response of the 4 (identical) Filters

10.4 Lessons Learned

The “Filter Grounding” experiments show that:

1. Filter grounding has a profound impact on the filter’s performance.
2. The filter ground must be connected to the return of its noise source.
3. The path of the filter’s input return to the noise source must be such that it does not couple inductively or capacitively to the filter’s output circuit. This is a delicate matter as the return of the input and output circuits are usually shared. Physically, it is the metal filter enclosure (for the selected filters here).
4. The wider the path to the ground plane, the better the separation between the filter’s input and output. Proper attention should also be given to the in- and output wire lengths: make these as short as possible.
5. The best way to mount a filter is to prevent coupling between the input and output circuits using a metal shield. In this board example, the output line is completely packaged within a metal enclosure. In the graph this way of shielding is called “Filter Plumbers Delight”, a terminology often used by radio amateurs.

Chapter 11

Discontinuities: Stubs

Contents

11.1 Demonstrations on the Discontinuities: Stubs Board

The Discontinuities: Stubs Board demonstrates the effects of discontinuities in the signal traces on a PCB. A change of width (impedance) and branching off is demonstrated.

11.2 Discontinuities: Stubs Board Views

11.2.1 The Finished Board

The end result of the assembly of the Discontinuities Stubs Board is shown in Figure 11.1

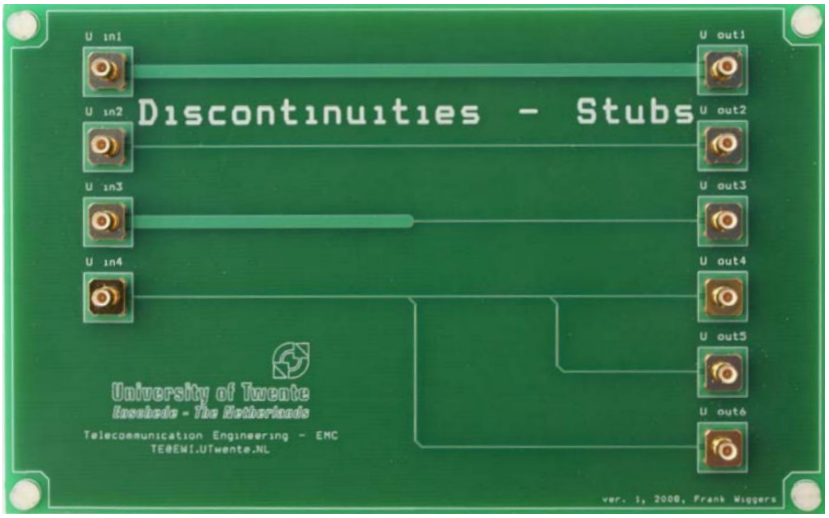

Figure 11.1: The Finished Discontinuities: Stubs Board.

11.2.2 The Silkscreen

The Silkscreen of the Discontinuities: Stubs Board shows where which components should be mounted:

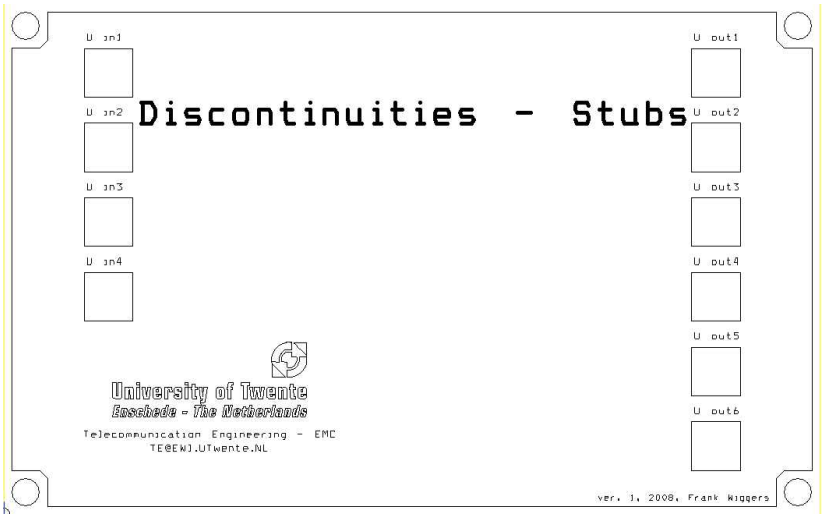

Figure 11.2: The Discontinuities: Stubs Board Silk Screen.

11.2.3 Bare Board Top View

The etch pattern of the empty board, seen from the top side, is shown in Figure 11.3.

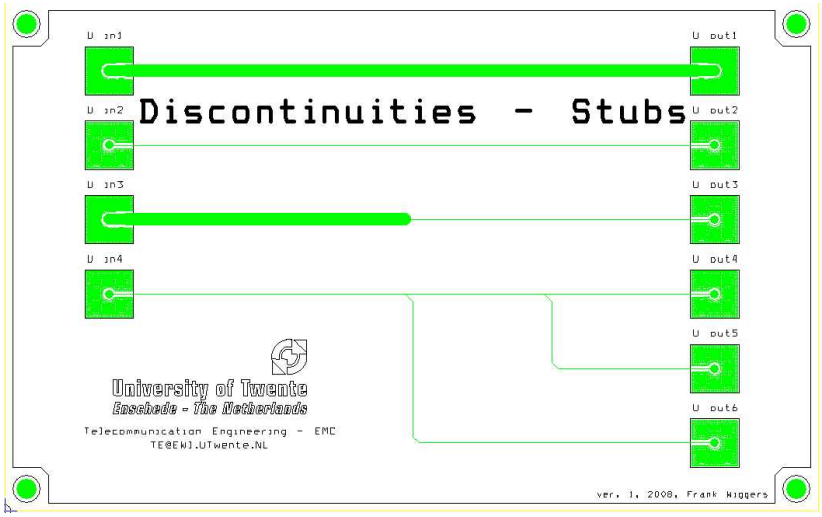

Figure 11.3: The Discontinuities: Stubs Bare Board (Top View)

11.2.4 Bare Board Bottom View

The etch pattern of the empty board, seen from the bottom side, is shown in Figure 11.4.

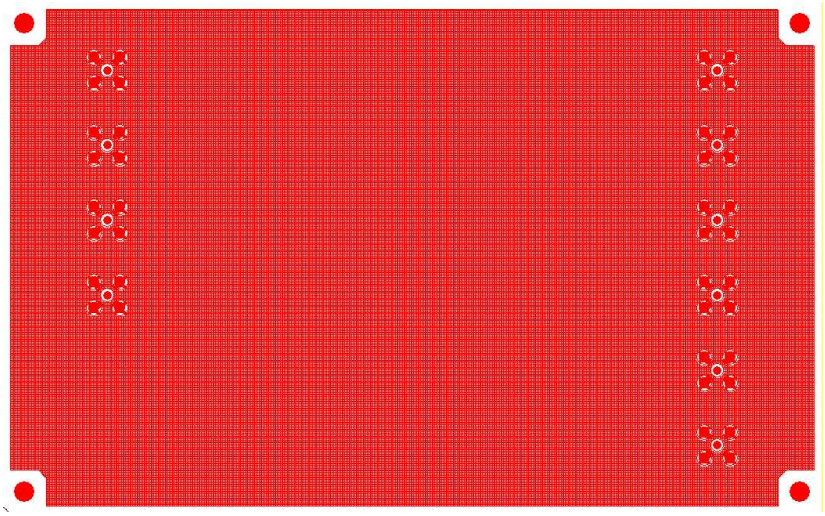

Figure 11.4: The Discontinuities: Stubs Board (Bottom View)

11.2.5 The Board Schematic

The schematic diagram of the Discontinuities: Stubs Board is shown in Figure 11.5

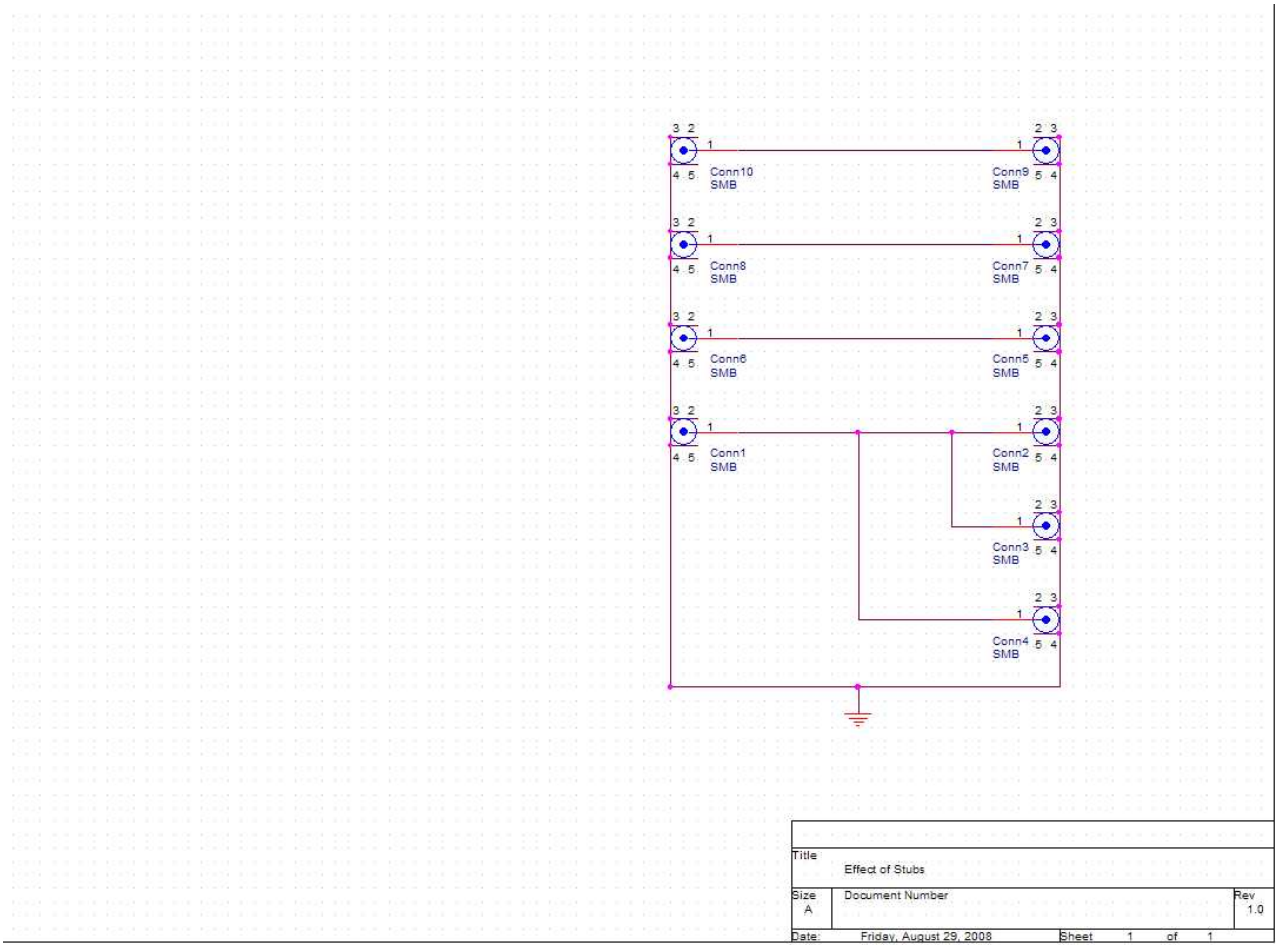

Figure 11.5: The Discontinuities: Stubs Board Schematic.

11.2.6 The Bill of Materials

The components to complete the Discontinuities: Stubs Board are shown in Table 11.1.

Table 11.1: Bill of Materials of the Discontinuities: Stubs Board

REF DES	VALUE	PACKAGE	FOOTPRINT
U in1	SMB	SMB	RF/SMB/V
U in2	SMB	SMB	RF/SMB/V
U in3	SMB	SMB	RF/SMB/V
U in4	SMB	SMB	RF/SMB/V
U out1	SMB	SMB	RF/SMB/V

Table 11.1: Bill of Materials of the Discontinuities: Stubs Board (cont'd)

REF DES	VALUE	PACKAGE	FOOTPRINT
U out2	SMB	SMB	RF/SMB/V
U out3	SMB	SMB	RF/SMB/V
U out4	SMB	SMB	RF/SMB/V
U out5	SMB	SMB	RF/SMB/V
U out6	SMB	SMB	RF/SMB/V

11.3 Board Functional Description

The “Discontinuities: Stubs” Board contains four individual interconnection traces over a ground plane: micro-striplines. Their performance over frequency is shown in Figure 11.6. To measure them, each line in turn is connected to a spectrum analyzer between the output of the tracking generator and the analyzer input. The response of the four traces (counting from the input connections) is shown, in the frequency domain, in Figure 11.6. Figure 11.6 shows that the effects below 100

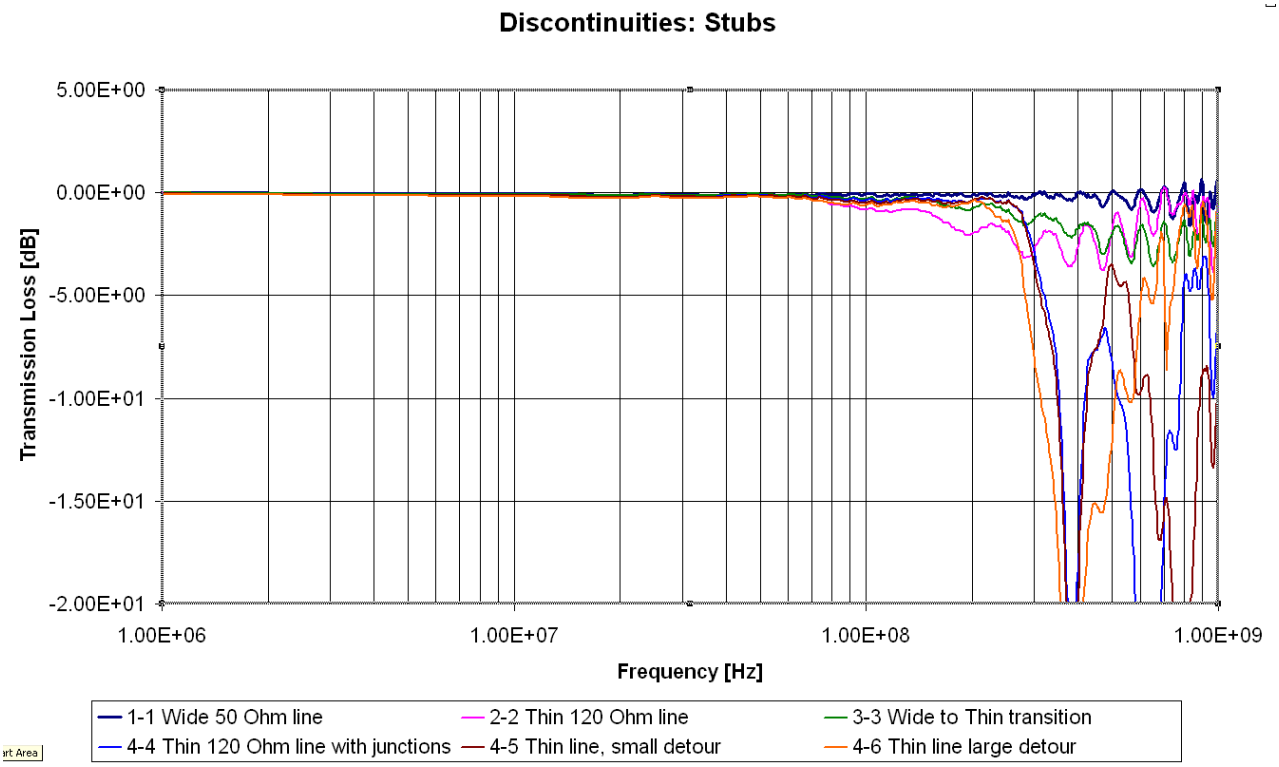

Figure 11.6: The Discontinuities: Stubs Interconnections Frequency Response

MHz are negligible. This is because the size of the interconnection structures are much smaller than the wavelength (which is 3 m for 100 MHz). When the frequencies go up, effects become visible. For the four cables the following observations can be made:

1. Trace 1 (between connector U in1 and U out1) is a 50Ω trace and minimally disturbs the impedance of the cables to and from the spectrum analyzer generator combination. The signal transmission is hence closest to the ideal 0 dB transmission loss line in Figure 11.6.

2. Trace 2 is a thin, 120Ω This implies that the impedances does not match the feeding lines. Reflections will occur and do affect the performance.

3. Trace 3 is a combination of line 1 and line 2. Up to half way, the line has a 50Ω impedance. The other half is a 120Ω line. Here reflections do occur. The disturbance is shorter and the impact slightly less than in line 2.

4. Trace 4 is different. Here a 120Ω line is split underway to form two separate arms. Each junction forms an impedance jump on the line. These junctions cause reflections as do the

ends of the line at the connectors. Due to the different locations of these reflection points, the reflected signals have different phases and have an tendency to cancel at specific frequencies (the deep valleys in the outputs measured at U out4, 5 and 6).

The same effects can also be observed in the time domain. A fast Time Domain Reflectometer is needed as individual reflections can only be seen if the rise time of the built in generator is shorter than the propagation delay of the line segment to be measured.

11.4 Lessons Learned

The “Discontinuities: Stubs” experiments show that:

1. Ideally, the impedance of a PCB trace should be equal to the feeding source and following load. For 50Ω the trace U in1 - U out1 is best.
2. If the impedance of the line differs from the source and/or load impedance, reflections will occur and the characteristics of the line will be less than ideal. Ideal for an interconnection means: 0 dB attenuation over the frequency range of interest. Example: the 120Ω line between U in2 and U out2, when driven and loaded by 50Ω.
3. The amount of signal distortion depends on the length of the mismatched line section (e.g. U in3 to U out3).
4. A high speed interconnection should never be split up into several line segments. Use a “Daisy Chain” instead! At the junction into two equal lines, the impedance drops a factor of two, causing reflections. Unequal stub lengths after the junction cause phase differences in the reflections that generate resonances (valleys) at specific frequencies.

Chapter 12

Discontinuities: Ground Apertures

Contents

12.1 Demonstrations on the Discontinuities: Ground Apertures Board

The Discontinuities: Ground Slots Board demonstrates the effects of irregularities in the signal return paths/planes on a PCB. The effect of a wide gap in the groundplane under a trace is shown. The discontinuity can be "repaired" by switching in parallel ground traces (direct and capacitive). The behavior of a trace over a narrow ground aperture can be compared to that of a trace over a wide ground plane.

12.2 Discontinuities: Ground Apertures Board Views

12.2.1 The Finished Board

The end result of the assembly of the Discontinuities: Ground Apertures Board is shown in Figure 12.1

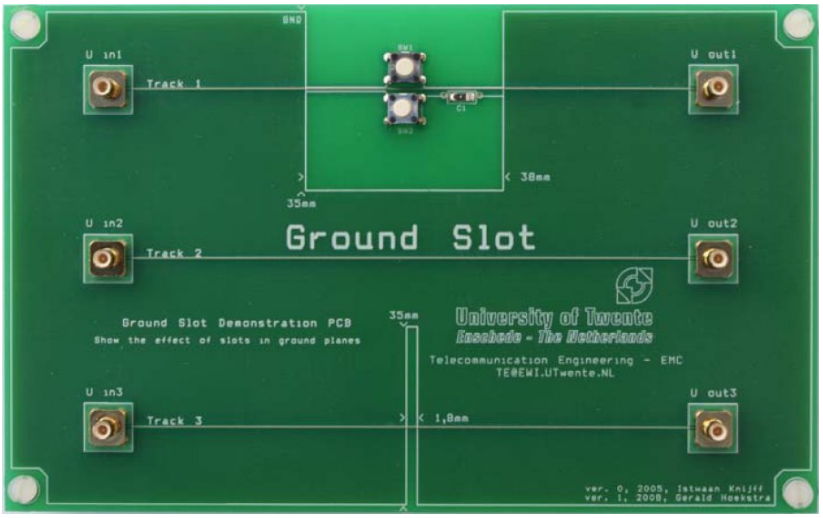

Figure 12.1: The Finished Discontinuities: Ground Apertures Board.

12.2.2 The Silkscreen

The Silkscreen of the Discontinuities: Ground Apertures Board shows where which components should be mounted:

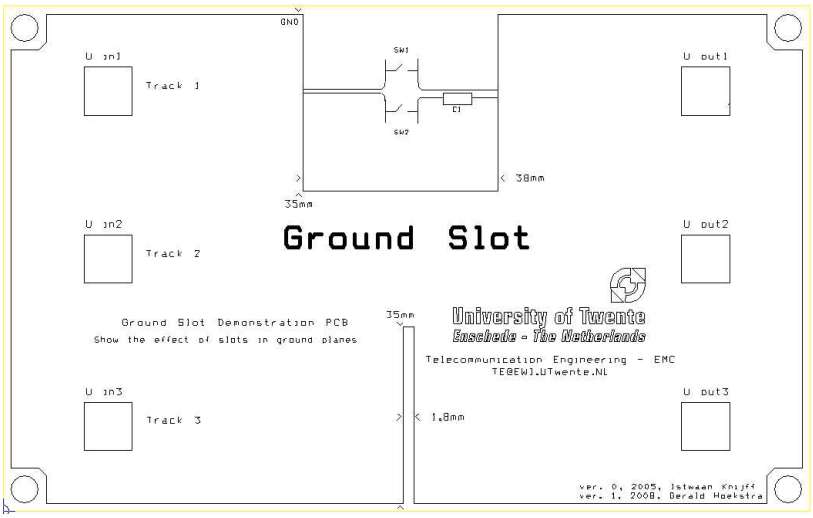

Figure 12.2: The Discontinuities: Ground Apertures Board Silk Screen.

12.2.3 Bare Board Top View

The etch pattern of the empty board, seen from the top side, is shown in Figure 12.3.

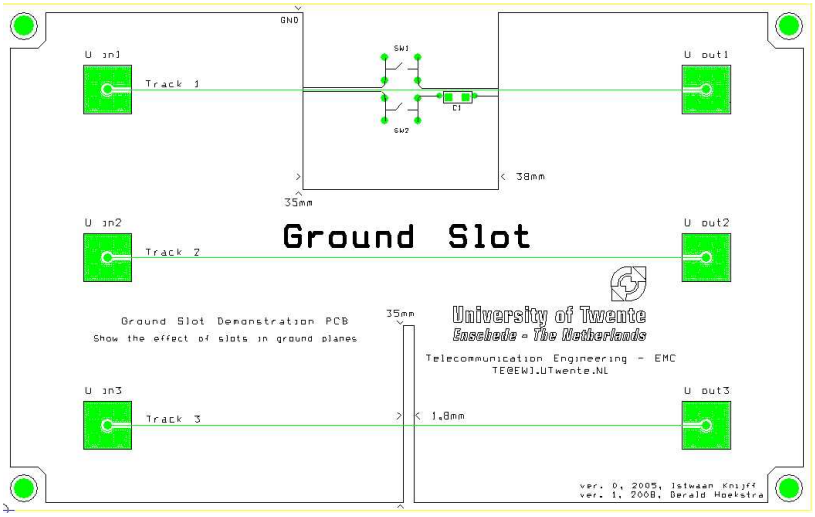

Figure 12.3: The Discontinuities: Ground Apertures Bare Board (Top View)

12.2.4 Bare Board Bottom View

The etch pattern of the empty board, seen from the bottom side, is shown in Figure 12.4.

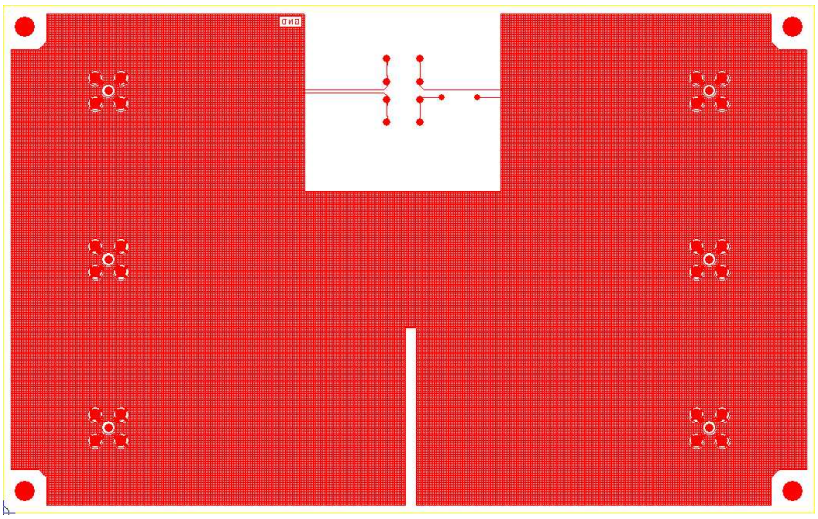

Figure 12.4: The Discontinuities: Ground Apertures Bare Board (Bottom View)

12.2.5 The Board Schematic

The schematic diagram of the Discontinuities: Ground Apertures Board is shown in Figure 12.5

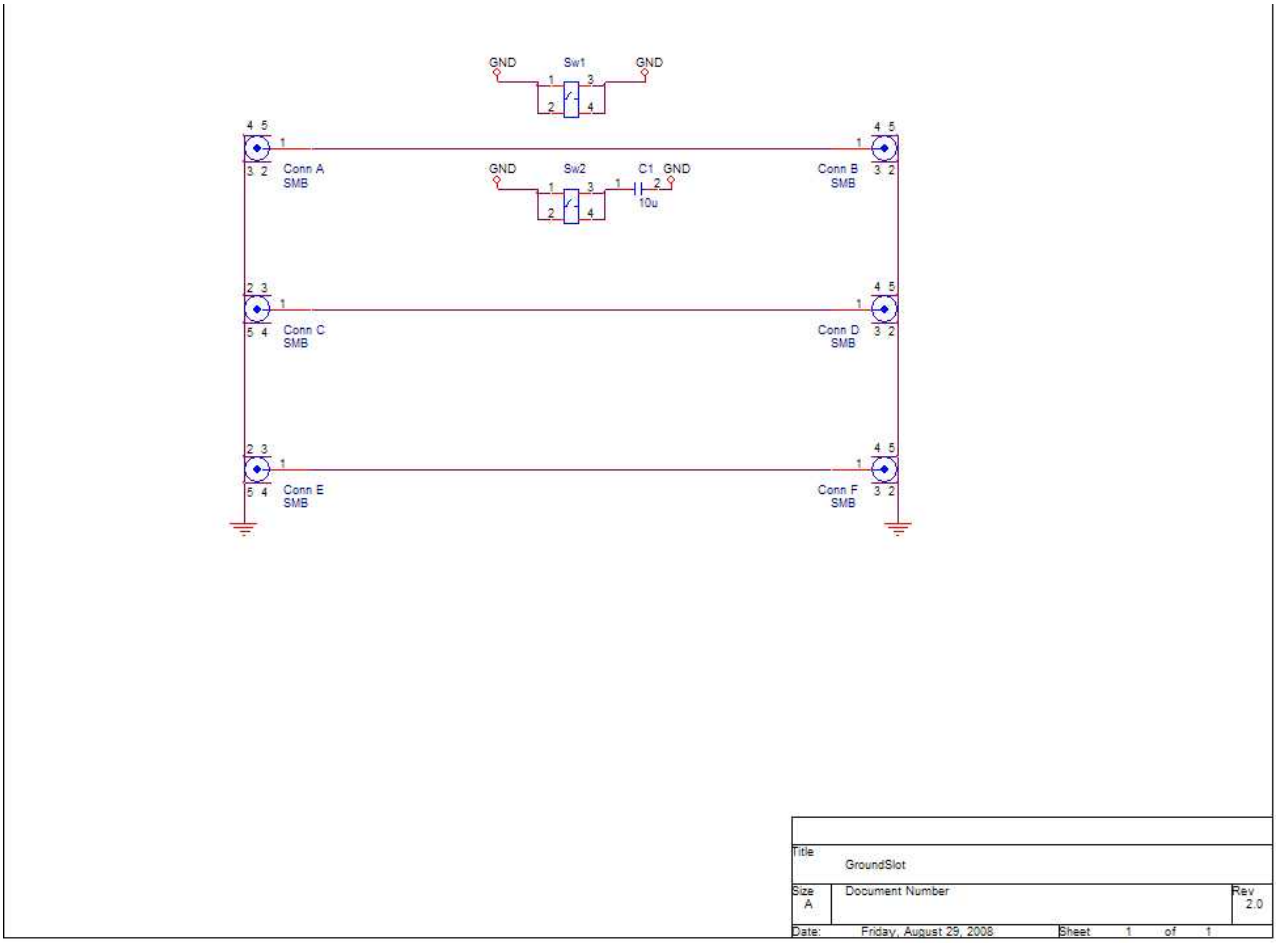

Figure 12.5: The Discontinuities: Ground Apertures Board Schematic.

12.2.6 The Bill of Materials

The components to complete the Discontinuities: Ground Apertures Board are shown in Table 12.1.

Table 12.1: Bill of Materials of the Discontinuities: Ground Apertures Board

REF DES	VALUE	PACKAGE	FOOTPRINT
U in1	SMB	SMB	RF/SMB/V
U in2	SMB	SMB	RF/SMB/V
U in3	SMB	SMB	RF/SMB/V
U out1	SMB	SMB	RF/SMB/V

Table 12.1: Bill of Materials of the Discontinuities: Ground Apertures Board (cont'd)

REF DES	VALUE	PACKAGE	FOOTPRINT
U out2	SMB	SMB	RF/SMB/V
U out3	SMB	SMB	RF/SMB/V
SW1	CON4_8	CON4_9	SWITCH-4PIN-TYCO-FSM4JH
SW2	CON4_8	CON4_9	SWITCH-4PIN-TYCO-FSM4JH
C1	100 nF	CAP_NP	SM/C_1206

12.3 Board Functional Description

The "Ground Stubs" Board has three identical traces with an impedance of approximately 120Ω. That implies that it will have reflections if sourced and loaded with 50Ω equipment. As a way to circumvent this, trace 2, between connectors U in2 and U out2, is connected to a (50Ω) spectrum analyzer - tracking generator combination. Initially, the generator is connected directly to the analyzer and calibrated to 0 dB. Then trace 2 is installed in between. The result is shown in Figure 12.6, the blue "Trace 2 Uncal". The the analyzer generator combination is calibrated again with trace 2 inserted. After that action, the trace 2 response shows as the green line "Trace 2 Cal" in Figure 12.6. To this line the other two traces will be compared. Trace 1 is routed over a wide ground plane aperture of 38 by 35 mm. If trace 1 is measured without pressing any of the switches, the graph in Figure 12.7, "Trace 1 Switches Open" appears. On the bottom of the board, under trace 1, two ground traces are routed. The one closest to the edge of the board can be switched on with switch SW1. If we press the SW1 button, the graph changes into the pink line "Trace 1 SW 1 Closed" in Figure 12.7. The other ground trace is switched by SW2, but it has an additional 100 nF capacitor in series. If SW2 is pressed, the green line in the graph "Trace 1 SW2 Closed" shows up. It lies exactly on top of the pink line found after switching SW1. This shows that, at these frequencies, a galvanic ground connection is not essential as long as there is a path for the return current. The improvement attained with these ground traces is not ideal: there is still a large loop present that resonates at 800 MHz. But, as the graphs show, the line can now be used up to 600 MHz with an attenuation of less than 2 dB instead of 100 MHz if the ground traces are left open! Trace 3 has a narrow ground aperture of 1.8 mm and a length of 35 mm. The attenuation graph is shown in Figure 12.8, as the red line "Trace 3 over Ground Slot". It is clear that the interconnection can be used up to about 1 GHz without to much attenuation. Above that frequency, the attenuation goes up rapidly. As an additional experiment a metal plate of 30 x 60 mm was placed under the board to (optically) cover the ground slot. As the board is covered with a solder-resist layer, this plate is only capacitively coupled. Nevertheless, the behavior of the trace is improved to the level of our reference trace 2. This is shown in Figure 12.8 by the green line "Trace 3 GND Slot Covered".

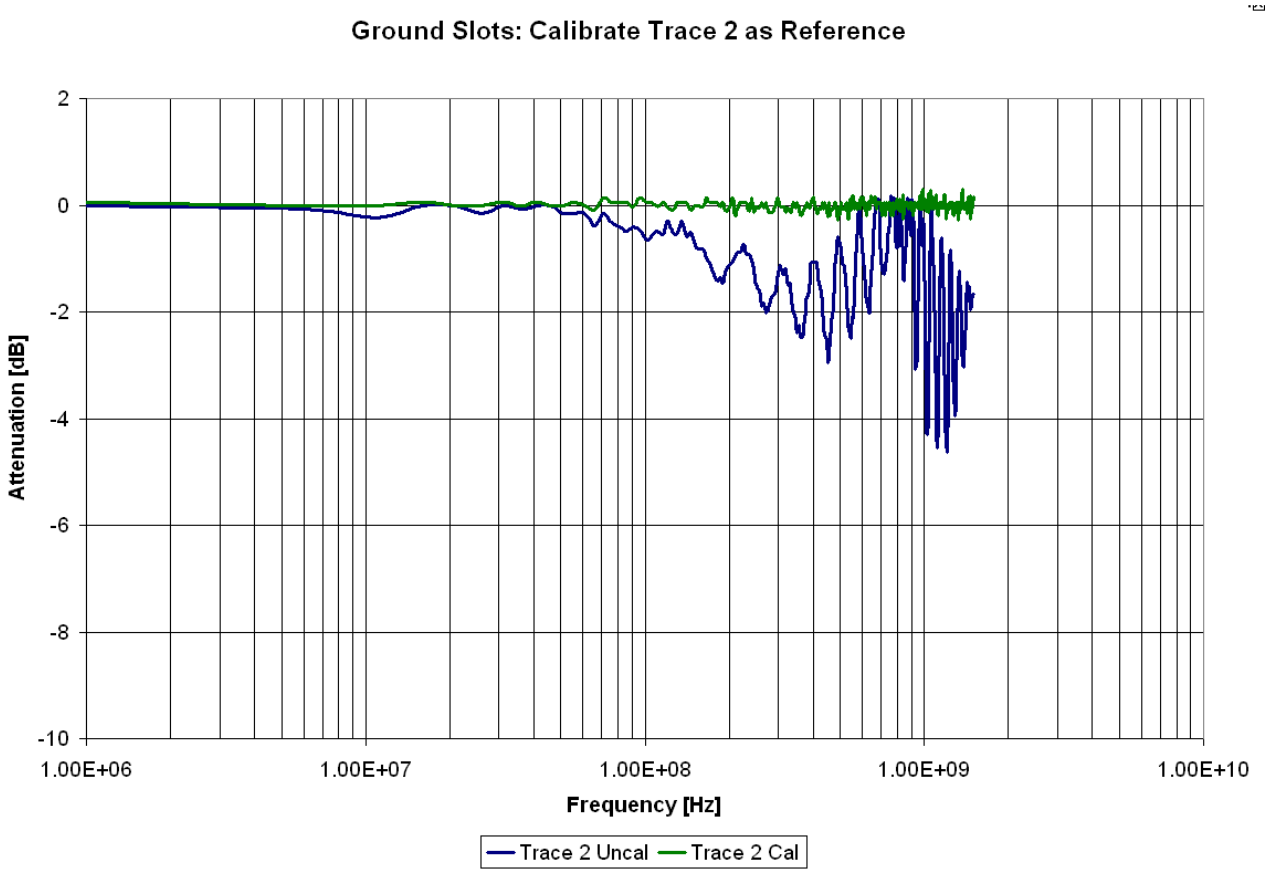

Figure 12.6: Trace 2 Calibrated as Reference in the Frequency Domain

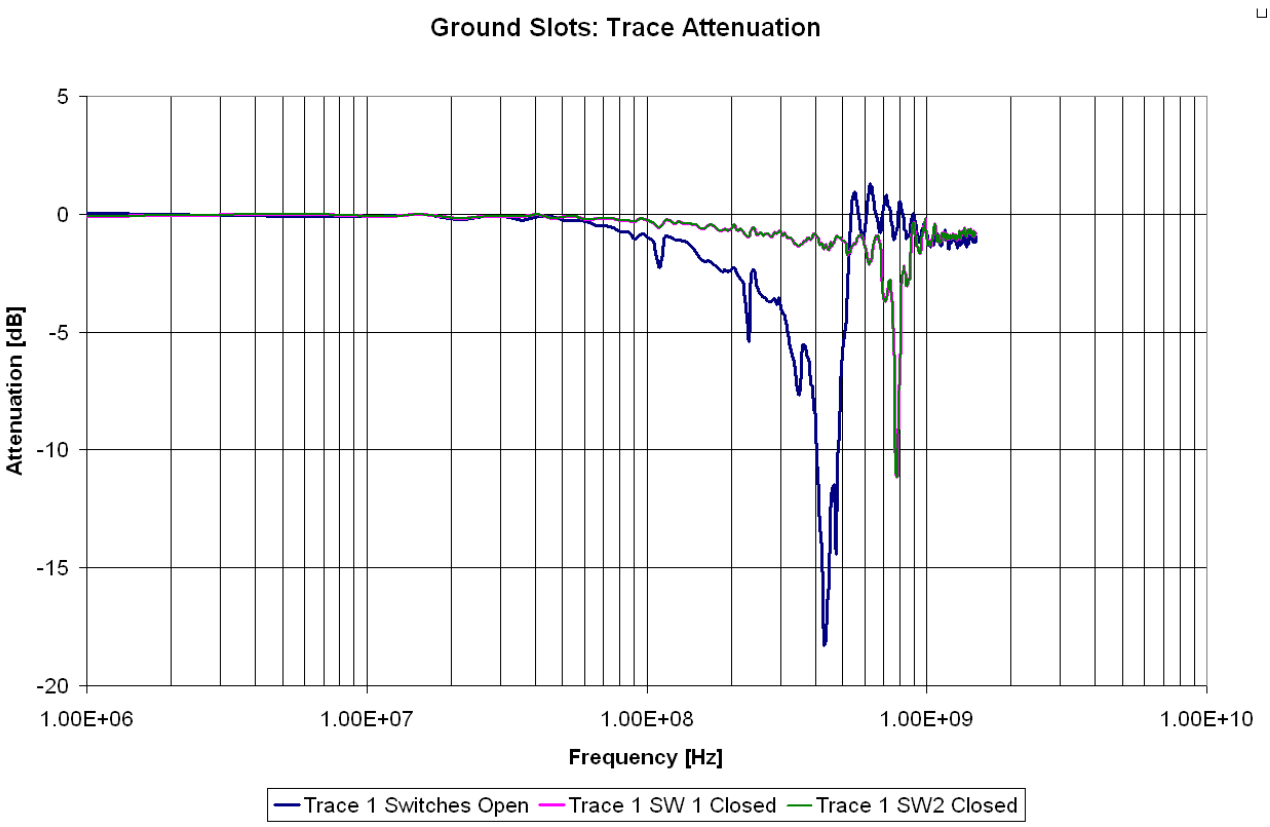

Figure 12.7: Frequency Responses of Trace 1 with and without Ground Return Traces

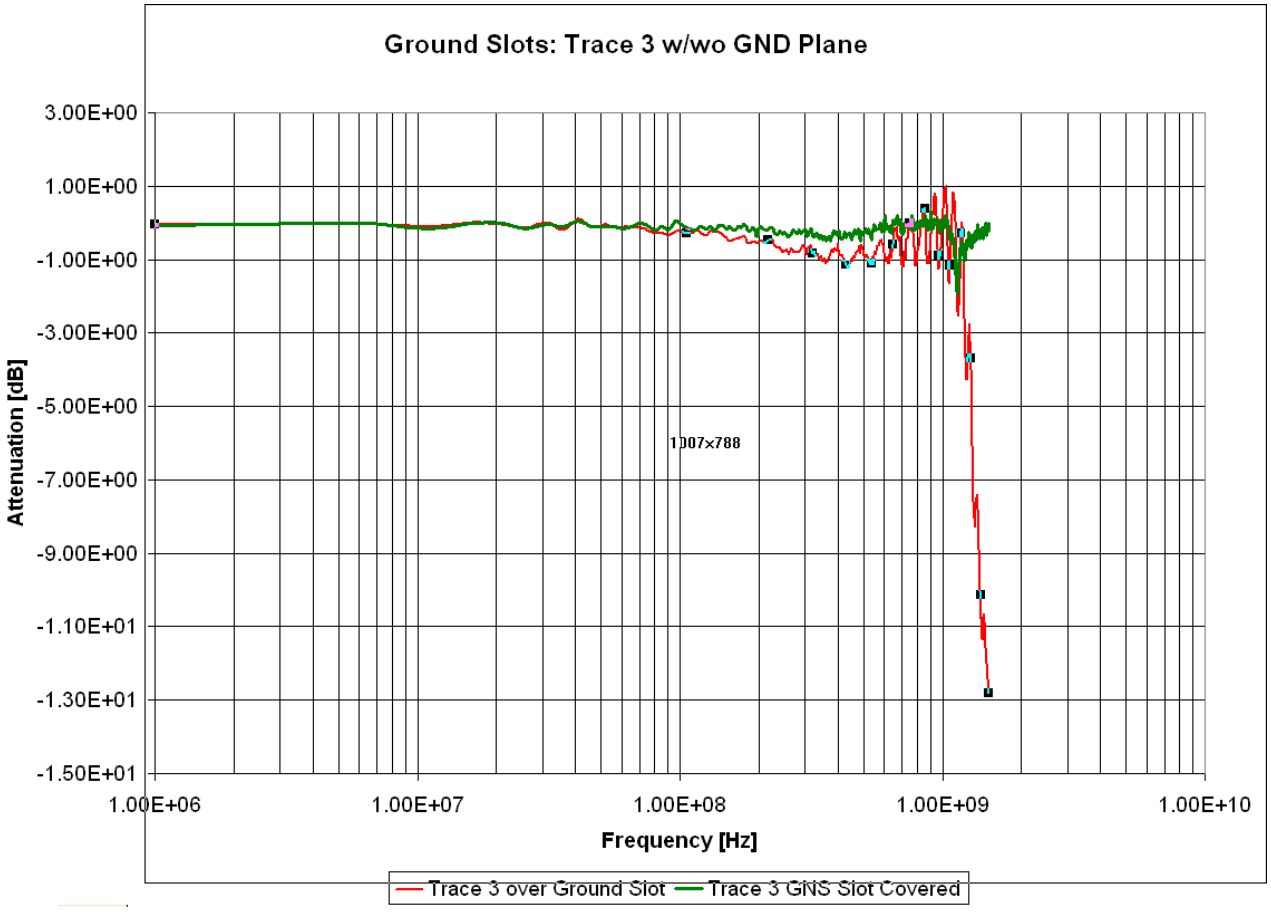

Figure 12.8: Frequency Response of Trace 3 with and without Capacitive Ground Plane under Slot

12.4 Lessons Learned

The “Discontinuities: Ground Apertures” experiments show that:

1. Apertures in the ground plane underneath signal traces greatly impairs the performance of the interconnection for high frequencies. The message is: do not route traces over return plane gaps.
2. The presence of a nearby ground return trace can greatly improve the performance, even if it has just the same width as the signal trace.
3. It is not necessary to connect a ground trace (or strip, we still prefer wide grounds) galvanically. A capacitive connection is sufficient. This can be useful if the two return planes do not have the same DC level (e.g. connecting Ground to a Vcc plane. The capacitive connection could be a capacitor or just capacitive overlap of the two planes. The latter solution is preferred if the planes are wide enough.
4. A gap in a ground plane can be covered with an insulated ground plane nearby. The overlap needed depends on the frequencies involved.

Chapter 13

Ground Bounce: Package Type

Contents

13.1 Demonstrations on the Ground Bounce: Package Type Board

The Ground Bounce: Package Type Board shows that large power current surges in a digital device due to simultaneous switching of outputs, causes a positive spike on the on-chip ground level with respect to the ground level on the Printed Circuit Board (PCB). This particular board has three identical chips in varying packages from TSSOP to DIL to see if this makes any difference.

13.2 Ground Bounce: Package Type Board Views

13.2.1 The Finished Board

The end result of the assembly of the Ground Bounce: Package Type Board is shown in Figure 13.1

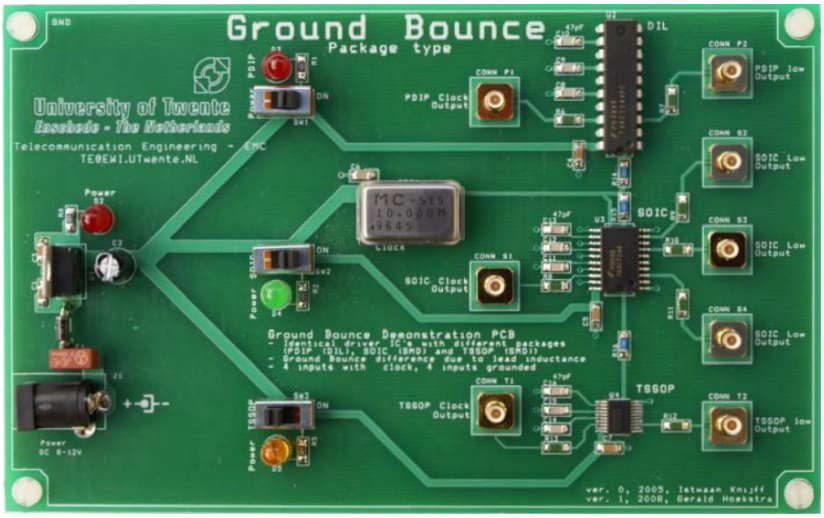

Figure 13.1: The Finished Ground Bounce: Package Type Board.

13.2.2 The Silkscreen

The Silkscreen of the Ground Bounce: Package Type Board shows where which components should be mounted:

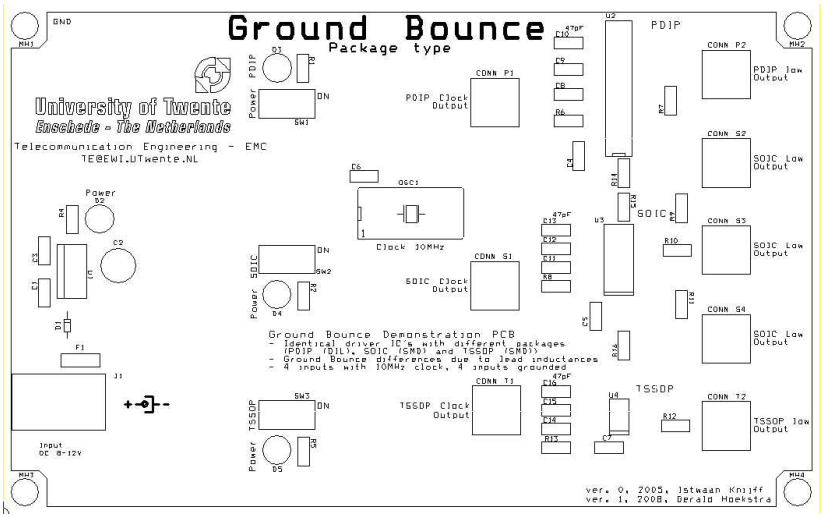

Figure 13.2: The Ground Bounce: Package Type Board Silk Screen.

13.2.3 Bare Board Top View

The etch pattern of the empty board, seen from the top side, is shown in Figure 13.3.

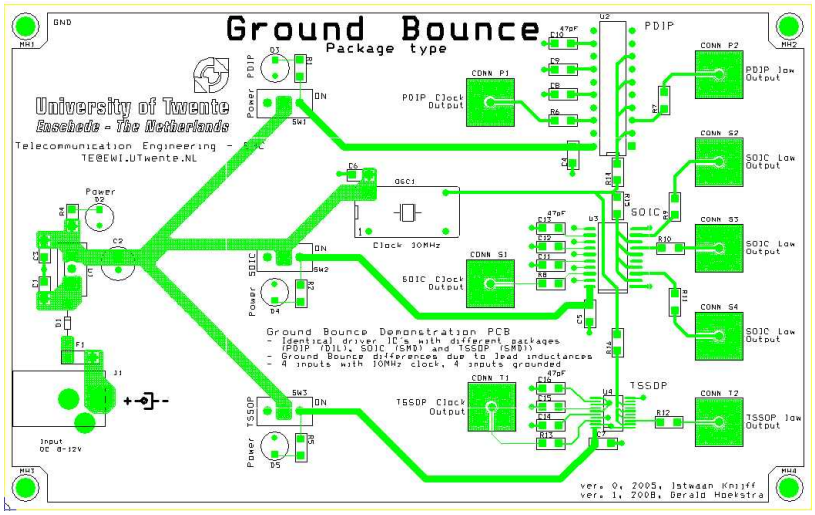

Figure 13.3: The Ground Bounce: Package Type Bare Board (Top View)

13.2.4 Bare Board Bottom View

The etch pattern of the empty board, seen from the bottom side, is shown in Figure 13.4.

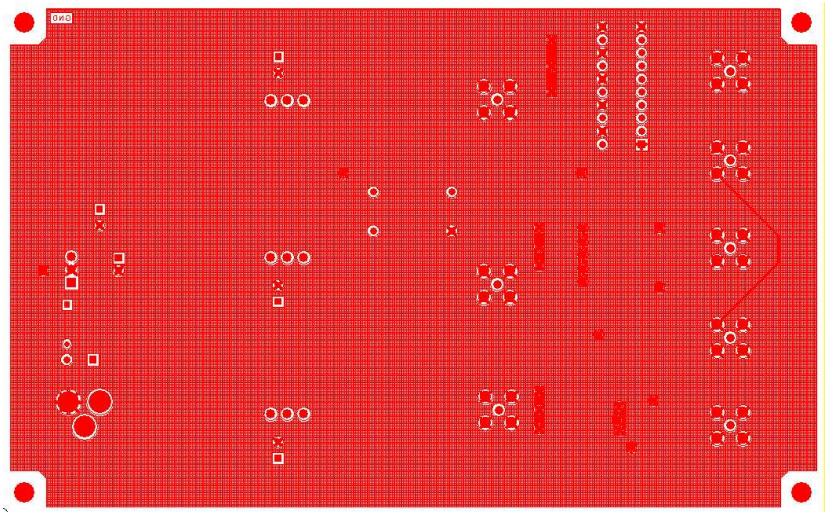

Figure 13.4: The Ground Bounce: Package Type Bare Board (Bottom View)

13.2.5 The Board Schematic

The schematic diagram of the Ground Bounce: Package Type Board is shown in Figure 13.5

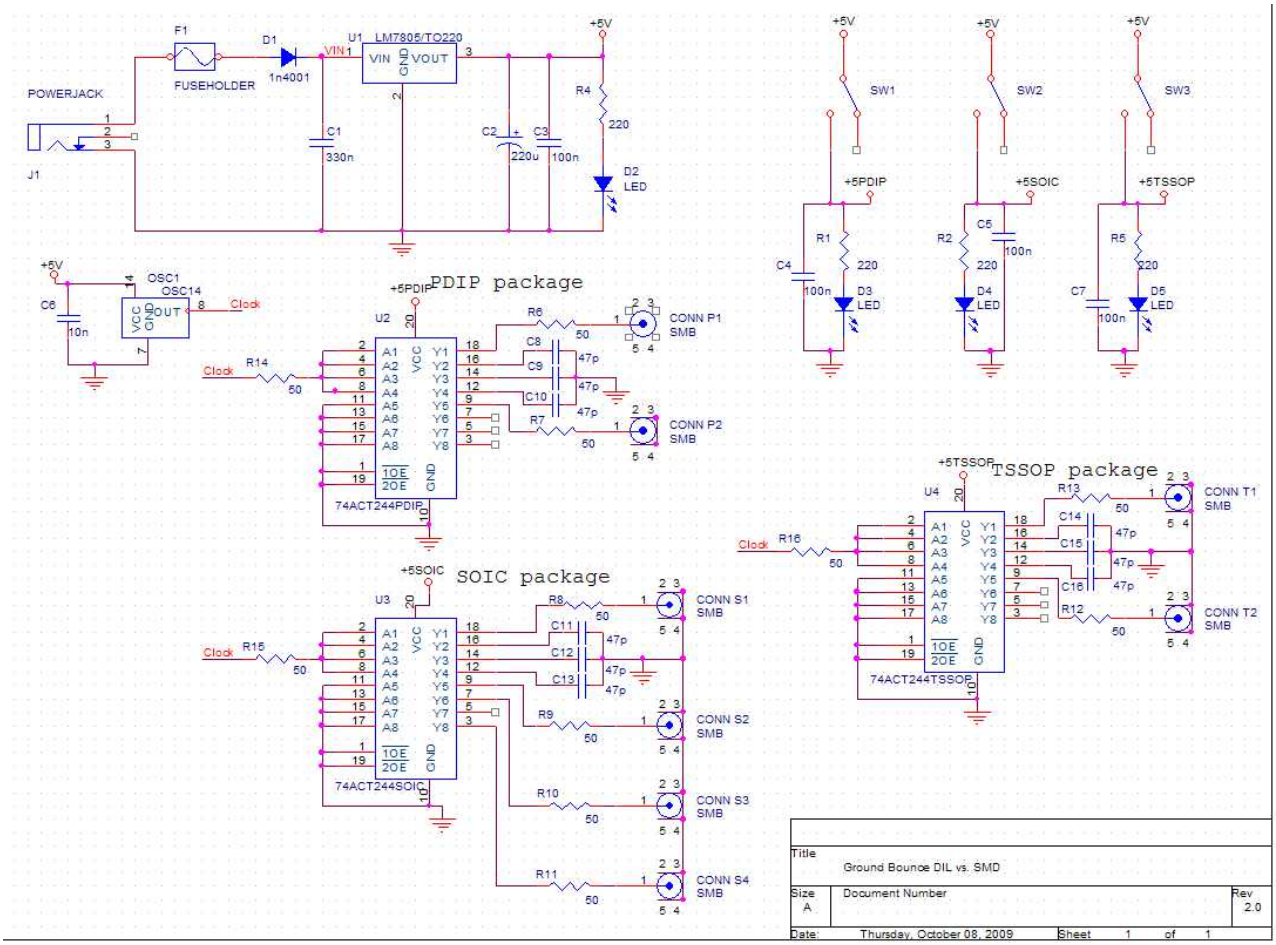

Figure 13.5: The Ground Bounce: Package Type Board Schematic.

13.2.6 The Bill of Materials

The components to complete the Ground Bounce: Package Type Board are shown in Table 13.1.

Table 13.1: Bill of Materials of the Ground Bounce: Package Type Board

REF DES	VALUE	PACKAGE	FOOTPRINT
C1	330n	CAP_NP	SM/C_1206
C2	220u	CAP_POL_0	CYL/D.275/LS.100/.034
C3	100n	CAP_NP	SM/C_1206
C4	100n	CAP_NP	SM/C_1206
C5	100n	CAP_NP	SM/C_1206

Table 13.1: Bill of Materials of the Ground Bounce: Package Type Board (cont'd)

REF DES	VALUE	PACKAGE	FOOTPRINT
C6	10n	CAP_NP	SM/C_1206
C7	100n	CAP_NP	SM/C_1206
C8	47p	CAP_NP	SM/C_1206
C9	47p	CAP_NP	SM/C_1206
C10	47p	CAP_NP	SM/C_1206
C11	47p	CAP_NP	SM/C_1206
C12	47p	CAP_NP	SM/C_1206
C13	47p	CAP_NP	SM/C_1206
C14	47p	CAP_NP	SM/C_1206
C15	47p	CAP_NP	SM/C_1206
C16	47p	CAP_NP	SM/C_1206
CONN P1	SMB	SMB	RF/SMB/V
CONN P2	SMB	SMB	RF/SMB/V
CONN S1	SMB	SMB	RF/SMB/V
CONN S2	SMB	SMB	RF/SMB/V
CONN S3	SMB	SMB	RF/SMB/V
CONN S4	SMB	SMB	RF/SMB/V
CONN T1	SMB	SMB	RF/SMB/V
CONN T2	SMB	SMB	RF/SMB/V
D1	1n4001	DIODE_0	DAX2/.300X.050/.028
D2	LED RED	LED	CYL/D.225/LS.125/.031
D3	LED RED	LED	CYL/D.225/LS.125/.031
D4	LED GRN	LED	CYL/D.225/LS.125/.031
D5	LED YEL	LED	CYL/D.225/LS.125/.031
F1	FUSEHOLDER	FUSEHOLDER	BLKCON.200/VH/TM1SQ/W.100/2
J1	POWERJACK	PHONEJACK_0	POWERJACK
OSC1	10 MHz	OSC14	OSC
R1	220	RESISTOR	SM/R_1206
R2	220	RESISTOR	SM/R_1206
R4	220	RESISTOR	SM/R_1206
R5	220	RESISTOR	SM/R_1206
R6	50	RESISTOR	SM/R_1206
R7	50	RESISTOR	SM/R_1206
R8	50	RESISTOR	SM/R_1206
R9	50	RESISTOR	SM/R_1206
R10	50	RESISTOR	SM/R_1206
R11	50	RESISTOR	SM/R_1206
R12	50	RESISTOR	SM/R_1206
R13	50	RESISTOR	SM/R_1206
R14	50	RESISTOR	SM/R_1206
R15	50	RESISTOR	SM/R_1206
R16	50	RESISTOR	SM/R_1206

Table 13.1: Bill of Materials of the Ground Bounce: Package Type Board (cont'd)

REF DES	VALUE	PACKAGE	FOOTPRINT
SW1	SW KEY-SPDT	SW_KEY-SPDT_1	SLIDESWITCH
SW2	SW KEY-SPDT	SW_KEY-SPDT_1	SLIDESWITCH
SW3	SW KEY-SPDT	SW_KEY-SPDT_1	SLIDESWITCH
U1	LM7805/TO220	L7805/TO220_2	TO220AB
U2	74ACT244PDIP	74ACT244	DIP.100/20/W.300/L1.050
U3	74ACT244SOIC	74ACT244	SOG.050/20/WG.420/L.500
U4	74ACT244TSSOP	74ACT244	SOG.65M/20/WG8.20/L6.98

13.3 Board Functional Description

The "Ground Bounce: Package Type" Board demonstrates the effect of large power currents due to the simultaneous switching of many outputs of e.g. a driver IC. This is shown in Figure 13.6.
On the "Ground Bounce: Package Type" Board the high currents in the output stages of a driver IC are generated by loading some of them with small capacitors (47 pF). Four outputs are switched with a 10 MHz clock. The other four remain at ground level. This same setup is made using three different IC Packages:

1. A "through hole" Dual In Line (DIL)
2. A Small Outline Integrated Circuit (SOIC)
3. A Thin Shrink Small Outline Package (TSSOP)

To operate the board, a power supply of 9 - 12 VDC is needed, center pin positive. We used a 9 V 1.33 A Switched Mode Model. By the way, diode D1 protects the board against wrong polarity! There is an LED to indicate the power supply circuit is working properly. The three IC's "under test" can be switched on and off individually using switches SW1 through SW3. LED's indicate the on/off state of each section. Several outputs have been brought out to an SMB connector to be monitored (see schematic diagram in Figure 12.5). A fast (at least 200 MHz bandwidth) oscilloscope is needed to see the details. In Figure 13.7 the measured signals are shown. The effects at some non switched outputs of the various IC's are also shown separately in Figure 13.8.

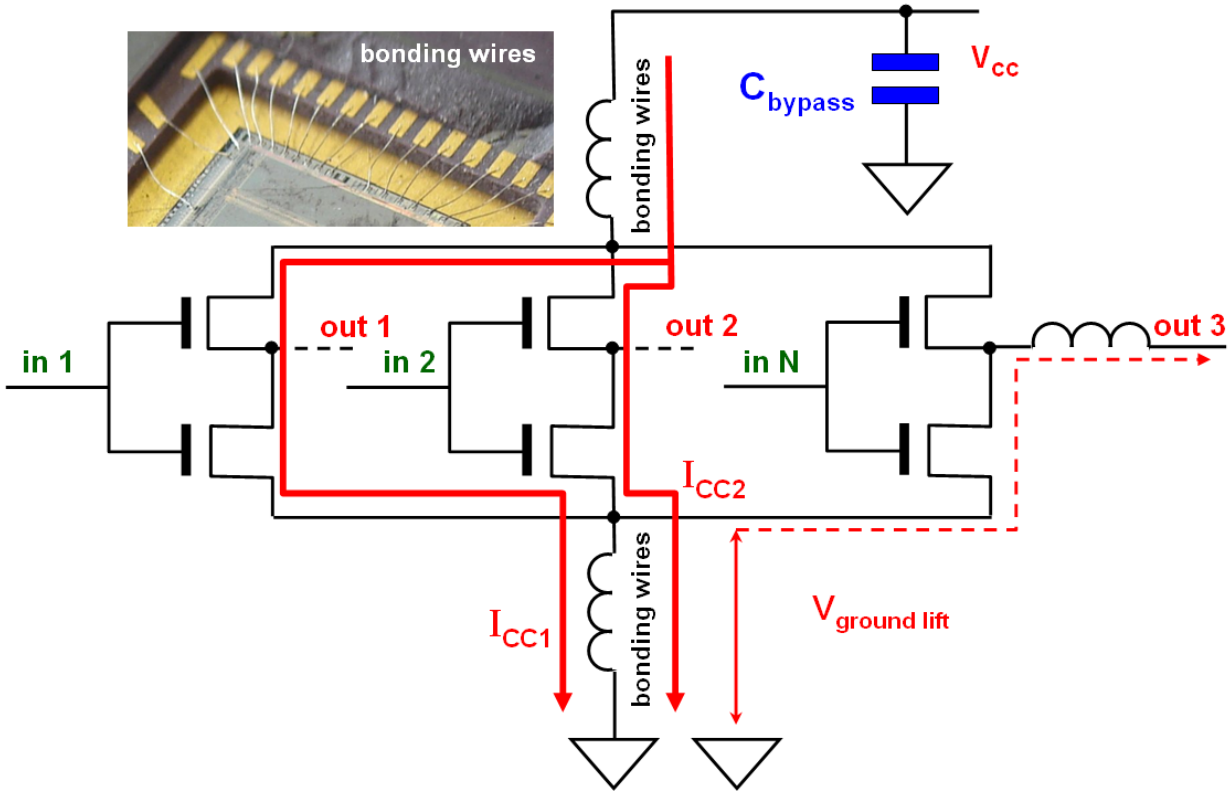

Figure 13.6: The Mechanism of Ground Bounce in an IC package

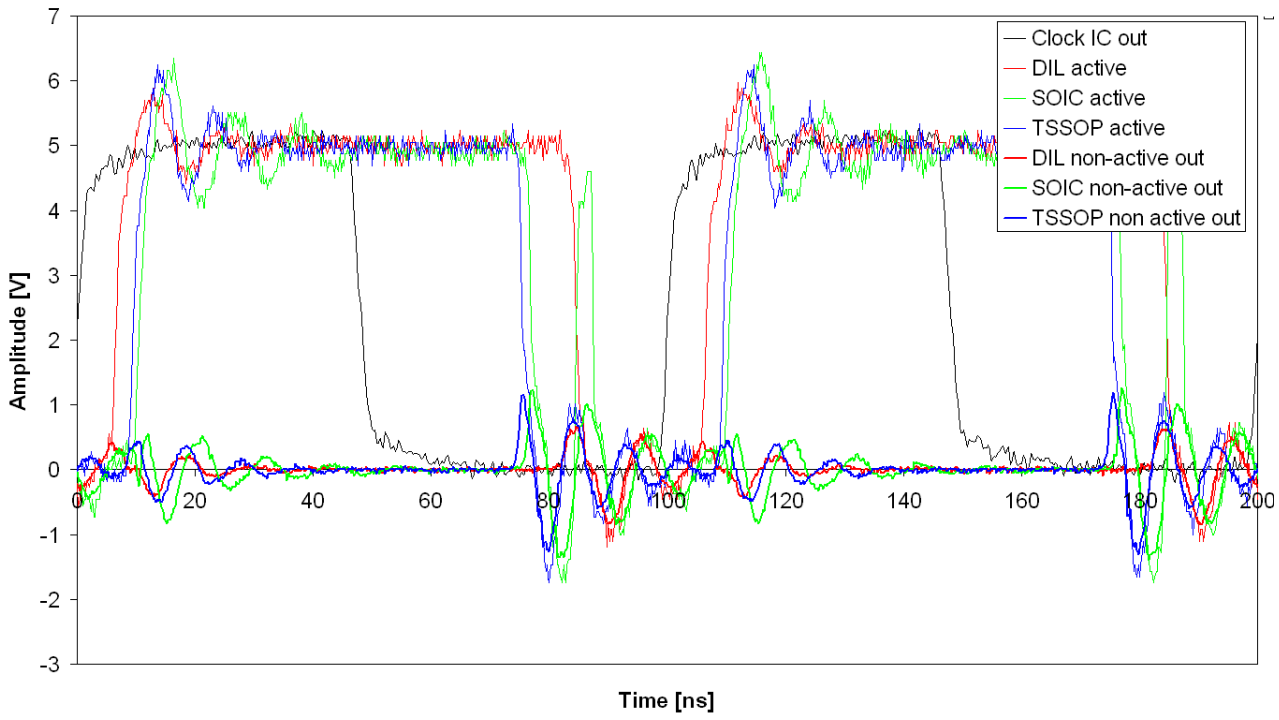

Figure 13.7: Signals Measured on Several IC Outputs

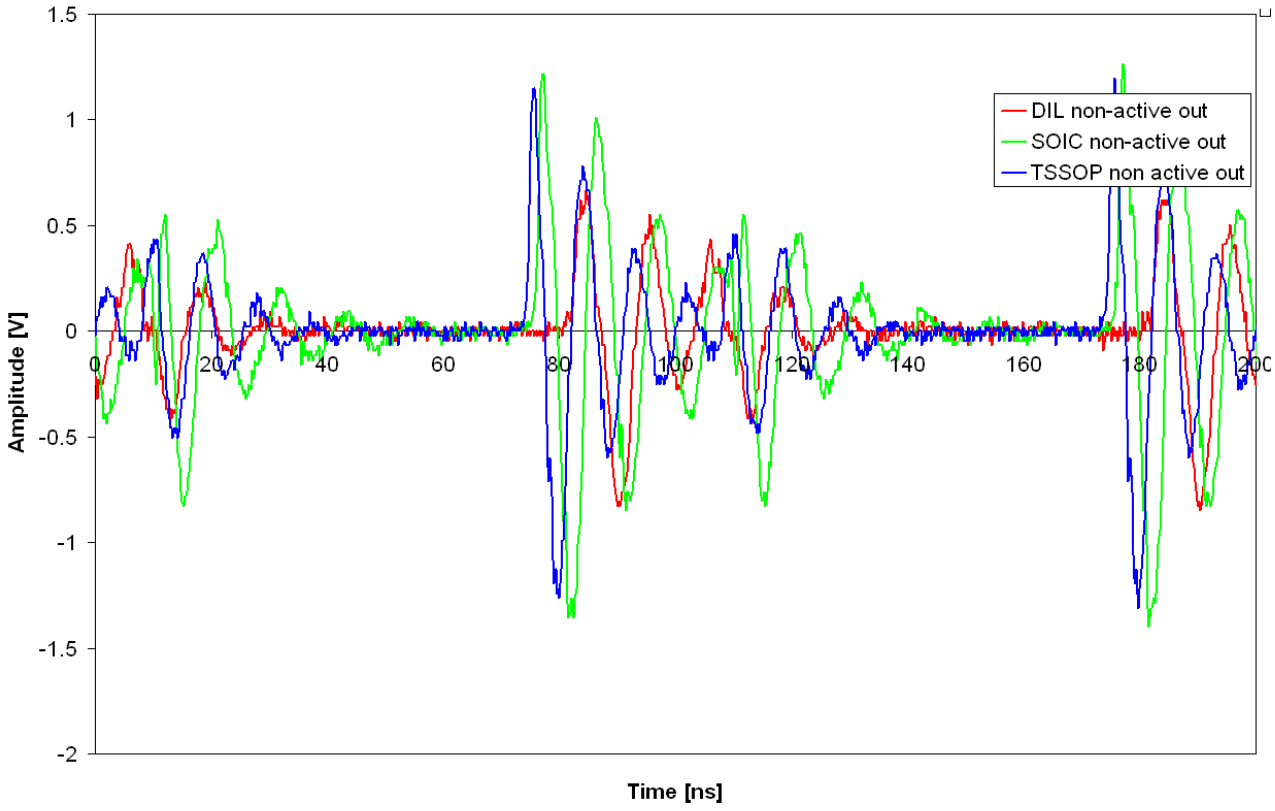

Figure 13.8: Ground Lift Spikes Measured on Several IC Outputs

13.4 Lessons Learned

The “Ground Bounce: Package Type” experiments show that:

1. Simultaneous switching of outputs of driver IC’s can lead to spiking on un-switched outputs. This Ground Bounce is an inductive effect over the bonding wires of the IC’s.
2. Choosing a smaller IC package may lead to a reduction of this effect.
3. Remember: the induction in the ground leads does not stop at the IC power pin. It may be continued to a noticeable degree if the board has long ground traces (instead of directly connecting to a wide power plane under the IC’s.

Chapter 14

Ground Bounce: Package Type Mk2

Contents

14.1 Demonstrations on the Ground Bounce: Package Type Board Mk2

The Ground Bounce: Package Type Board Mk2 shows that large power current surges in a digital device due to simultaneous switching of outputs, causes a positive spike on the on-chip ground level with respect to the ground level on the Printed Circuit Board (PCB). This particular board has three identical chips in varying packages from TSSOP to DIL to see if this makes any difference. This Mk2 version has an additional ground plane on the component side of the board to further improve (=reduce) the groundbounce effect.

14.2 Ground Bounce: Package Type Board Mk2 Views

14.2.1 The Finished Board

The end result of the assembly of the Ground Bounce: Package Type Mk2 Board is shown in Figure 14.1

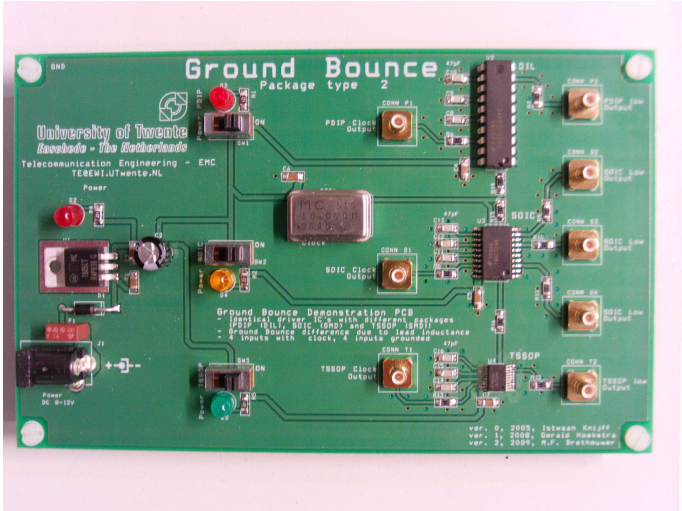

Figure 14.1: The Finished Ground Bounce: Package Type Mk2 Board.

14.2.2 The Silkscreen

The Silkscreen of the Ground Bounce: Package Type Mk2 Board shows where which components should be mounted:

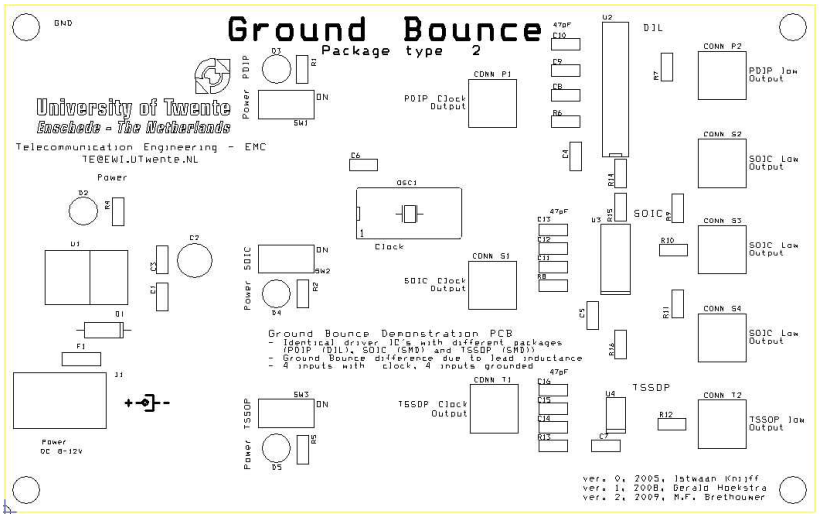

Figure 14.2: The Ground Bounce: Package Type Mk2 Board Silk Screen.

14.2.3 Bare Board Top View

The etch pattern of the empty Mk2 board, seen from the top side, is shown in Figure 14.3.

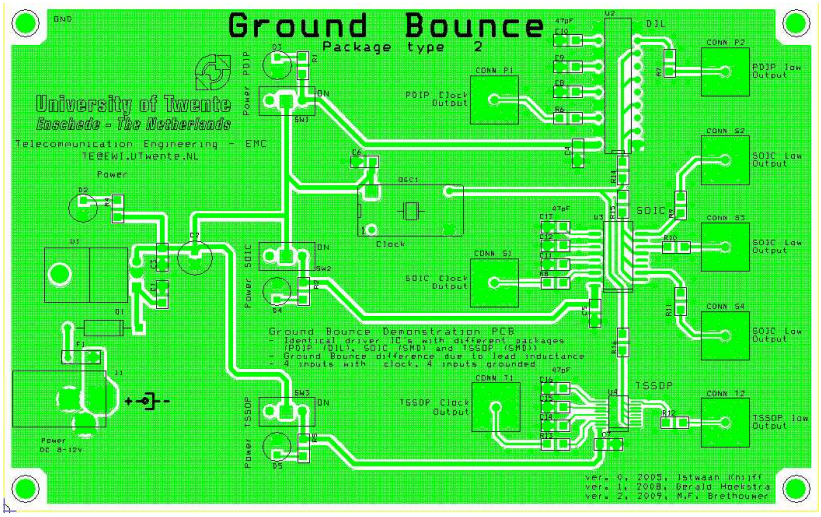

Figure 14.3: The Ground Bounce: Package Type Mk2 Bare Board (Top View)

14.2.4 Bare Board Bottom View

The etch pattern of the empty Mk2 board, seen from the bottom side, is shown in Figure 14.4.

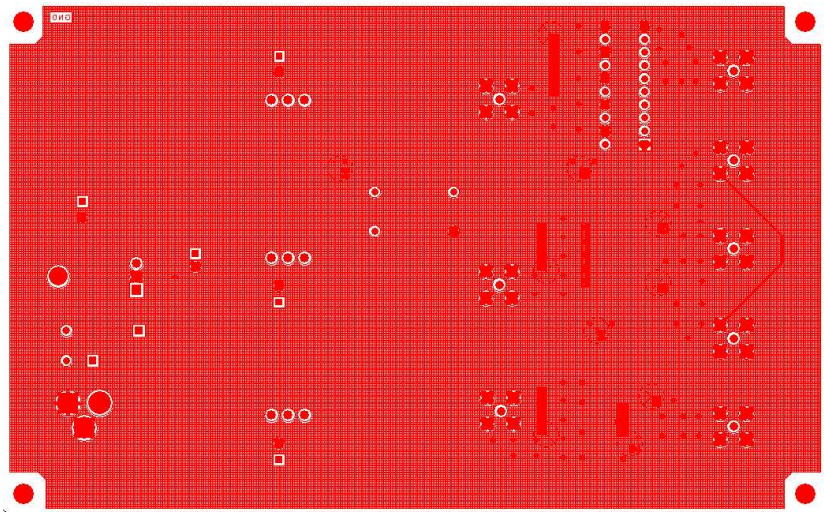

Figure 14.4: The Ground Bounce: Package Type Mk2 Bare Board (Bottom View)

14.2.5 The Board Schematic

The schematic diagram of the Ground Bounce: Package Type Mk2 Board is shown in Figure 14.5

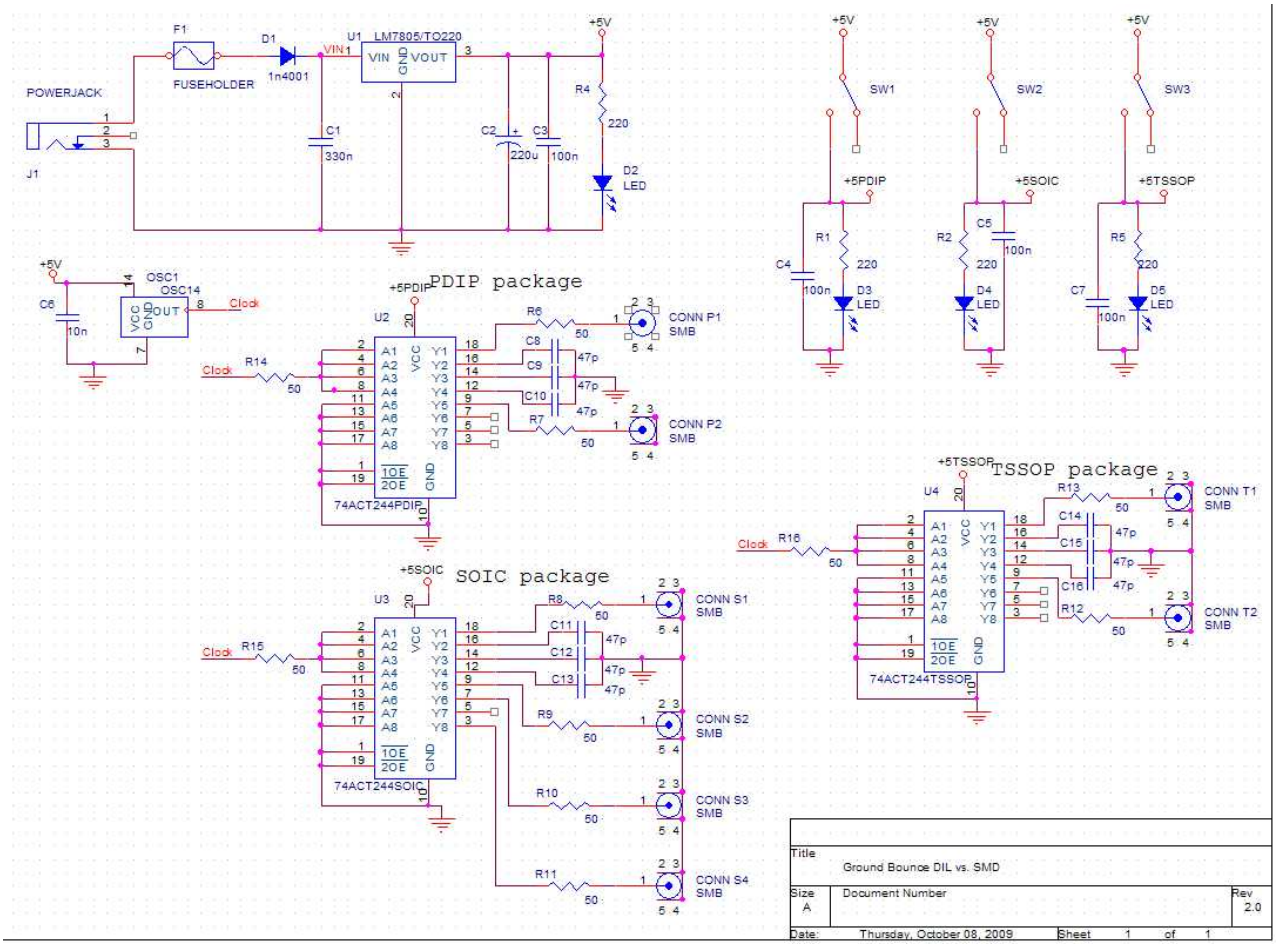

Figure 14.5: The Ground Bounce: Package Type Mk2 Board Schematic.

14.2.6 The Bill of Materials

The components to complete the Ground Bounce: Package Type Mk2 Board are shown in Table 14.1.

Table 14.1: Bill of Materials of the Ground Bounce: Package Type Mk2 Board

REF DES	VALUE	PACKAGE	FOOTPRINT
C1	330n	CAP_NP	SM/C_1206
C2	220u	CAP_POL_0	CYL/D.275/LS.100/.034
C3	100n	CAP_NP	SM/C_1206

Table 14.1: Bill of Materials of the Ground Bounce: Package Type Mk2 Board (cont'd)

REF DES	VALUE	PACKAGE	FOOTPRINT
C4	100n	CAP_NP	SM/C_1206
C5	100n	CAP_NP	SM/C_1206
C6	10n	CAP_NP	SM/C_1206
C7	100n	CAP_NP	SM/C_1206
C8	47p	CAP_NP	SM/C_1206
C9	47p	CAP_NP	SM/C_1206
C10	47p	CAP_NP	SM/C_1206
C11	47p	CAP_NP	SM/C_1206
C12	47p	CAP_NP	SM/C_1206
C13	47p	CAP_NP	SM/C_1206
C14	47p	CAP_NP	SM/C_1206
C15	47p	CAP_NP	SM/C_1206
C16	47p	CAP_NP	SM/C_1206
CONN P1	SMB	SMB	RF/SMB/V
CONN P2	SMB	SMB	RF/SMB/V
CONN S1	SMB	SMB	RF/SMB/V
CONN S2	SMB	SMB	RF/SMB/V
CONN S3	SMB	SMB	RF/SMB/V
CONN S4	SMB	SMB	RF/SMB/V
CONN T1	SMB	SMB	RF/SMB/V
CONN T2	SMB	SMB	RF/SMB/V
D1	1n4001	DIODE_0	DAX2/.300X.050/.028
D2	LED RED	LED	CYL/D.225/LS.125/.031
D3	LED RED	LED	CYL/D.225/LS.125/.031
D4	LED GRN	LED	CYL/D.225/LS.125/.031
D5	LED YEL	LED	CYL/D.225/LS.125/.031
F1	FUSEHOLDER	FUSEHOLDER	BLKCON.200/VH/TM1SQ/W.100/2
J1	POWERJACK	PHONEJACK_0	POWERJACK
OSC1	10 MHz	OSC14	OSC
R1	220	RESISTOR	SM/R_1206
R2	220	RESISTOR	SM/R_1206
R4	220	RESISTOR	SM/R_1206
R5	220	RESISTOR	SM/R_1206
R6	50	RESISTOR	SM/R_1206
R7	50	RESISTOR	SM/R_1206
R8	50	RESISTOR	SM/R_1206
R9	50	RESISTOR	SM/R_1206
R10	50	RESISTOR	SM/R_1206
R11	50	RESISTOR	SM/R_1206
R12	50	RESISTOR	SM/R_1206
R13	50	RESISTOR	SM/R_1206
R14	50	RESISTOR	SM/R_1206

Table 14.1: Bill of Materials of the Ground Bounce: Package Type Mk2 Board (cont'd)

REF DES	VALUE	PACKAGE	FOOTPRINT
R15	50	RESISTOR	SM/R_1206
R16	50	RESISTOR	SM/R_1206
SW1	SW KEY-SPDT	SW_KEY-SPDT_1	SLIDESWITCH
SW2	SW KEY-SPDT	SW_KEY-SPDT_1	SLIDESWITCH
SW3	SW KEY-SPDT	SW_KEY-SPDT_1	SLIDESWITCH
U1	LM7805/TO220	L7805/TO220_2	TO220AB
U2	74ACT244PDIP	74ACT244	DIP.100/20/W.300/L1.050
U3	74ACT244SOIC	74ACT244	SOG.050/20/WG.420/L.500
U4	74ACT244TSSOP	74ACT244	SOG.65M/20/WG8.20/L6.98

14.3 Board Functional Description

The "Ground Bounce: Package Type" Mk2 Board demonstrates the effect of large power currents due to the simultaneous switching of many outputs of e.g. a driver IC. As shown before in Figure 13.6 op Page 113. Apart from the extra ground plane on the component side, the operation of the board remains identical to that of the board without it, described in Chapter 13. Other (minor) improvements have led to differences in pin numbering, so a new schematic diagram is shown in Figure 14.5 for the Mk2 board.
On the "Ground Bounce: Package Type Mk2" Board the high currents in the output stages of a driver IC are generated by loading some of them with small capacitors (47 pF). Four outputs are switched with a 10 MHz clock. The other four remain at ground level. This same setup is made using three different IC Packages:

1. A "through hole" Dual In Line (DIL)
2. A Small Outline Integrated Circuit (SOIC)
3. A Thin Shrink Small Outline Package (TSSOP)

To operate the board, a power supply of 9 - 12 VDC is needed, center pin positive. We used a 9 V 1.33 A Switched Mode Model. By the way, diode D1 protects the board against wrong polarity! There is an LED to indicate the power supply circuit is working properly. The three IC's "under test" can be switched on and off individually using switches SW1 through SW3. LED's indicate the on/off state of each section. Several outputs have been brought out to an SMB connector to be monitored (see schematic diagram in Figure 14.5). A fast (at least 200 MHz bandwidth) oscilloscope is needed to see the details. In Figure 14.6 the measured signals are shown. The effects at some non switched outputs of the various IC's are also shown separately in Figure 14.7.

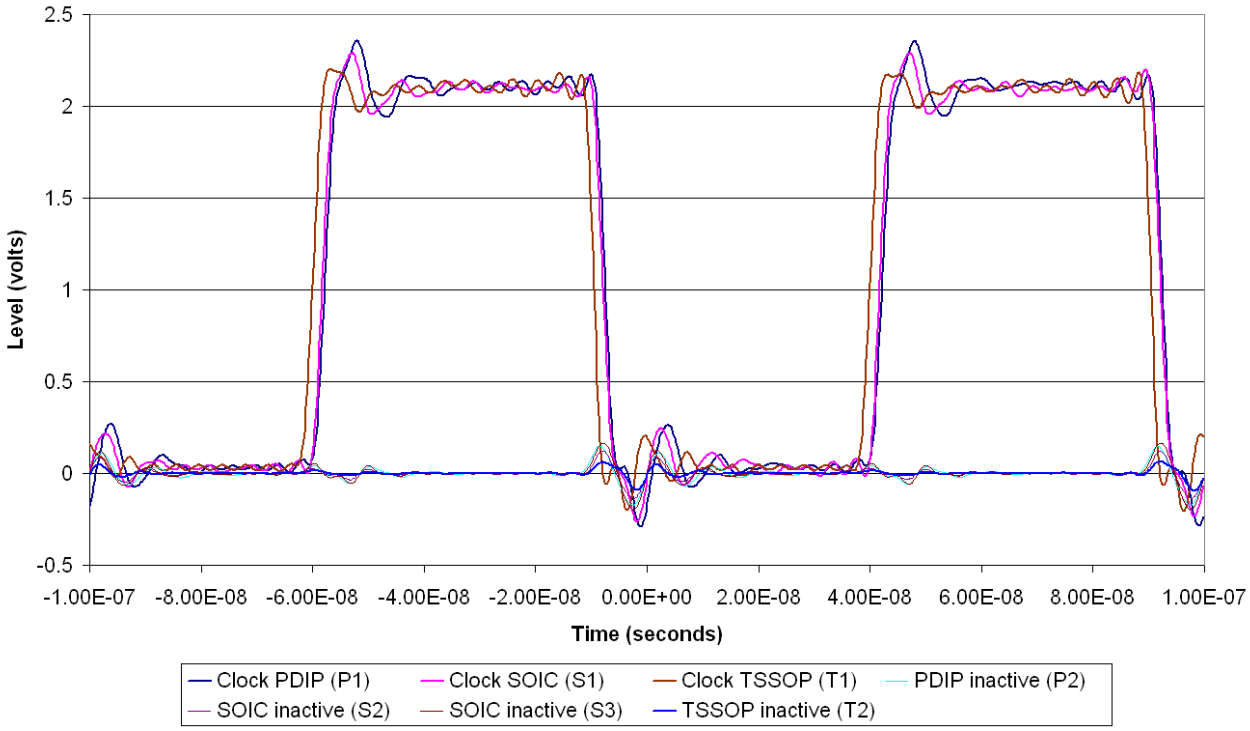

Figure 14.6: Signals Measured on Several IC Outputs

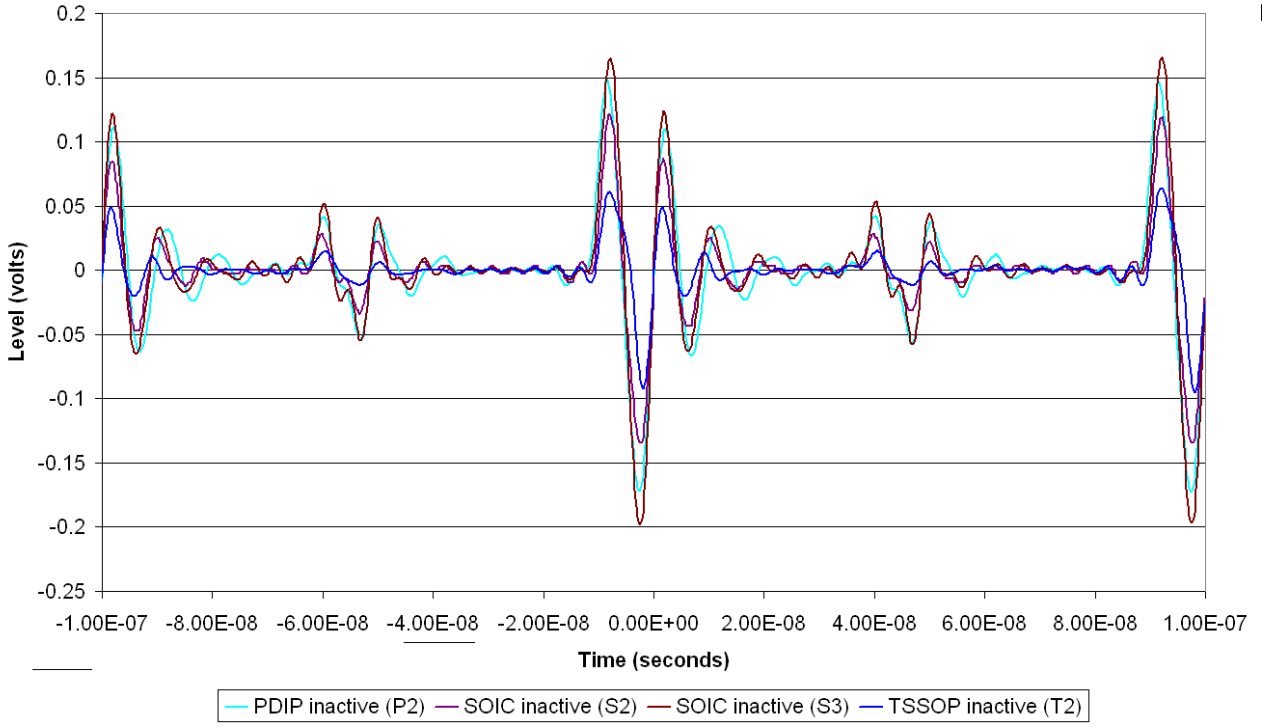

Figure 14.7: Ground Lift Spikes Measured on Several IC Outputs

14.4 Lessons Learned

The “Ground Bounce: Package Type” experiments show that:

1. Simultaneous switching of outputs of driver IC’s can lead to spiking on un-switched outputs. This Ground Bounce is an inductive effect over the bonding wires of the IC’s.
2. Choosing a smaller IC package may lead to a reduction of this effect.
3. Remember: the induction in the ground leads does not stop at the IC power pin. It may be continued to a noticeable degree if the board has long ground traces (instead of directly connecting to a wide power plane under the IC’s.

   And, for this Mk2 board:

4. Addition of an extra ground plane on the component side can help make the board ground connections shorter and hence reduce their inductance. This considerably reduces ground-bounce.

Chapter 15

Ground Bounce: Power Pinning

Contents

15.1 Demonstrations on the Ground Bounce: Power Pinning Board

The Ground Bounce: Power Pinning Board shows the same effect as the Ground Bounce Package Type Board but focusses on the difference between devices with end and center power pinning layout.

15.2 Ground Bounce: Power Pinning Board Views

15.2.1 The Finished Board

The end result of the assembly of the Ground Bounce: Power Pinning Board is shown in Figure 15.1

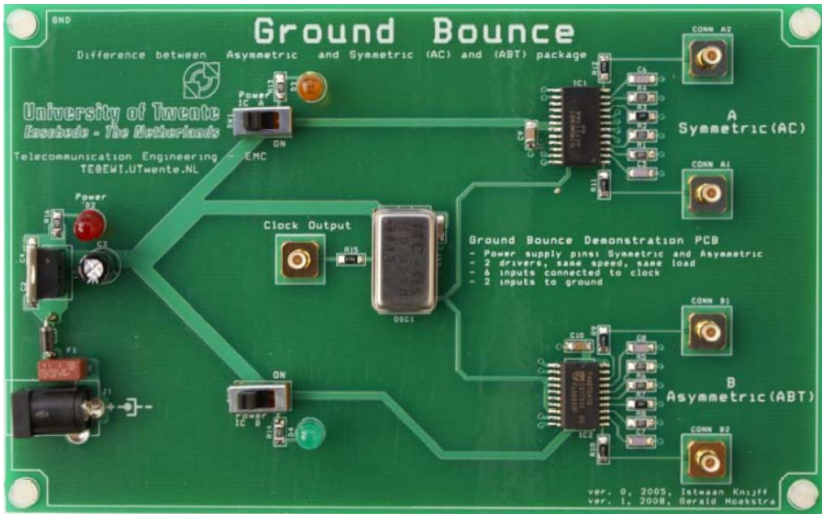

Figure 15.1: The Finished Ground Bounce: Power Pinning Board.

15.2.2 The Silkscreen

The Silkscreen of the Ground Bounce: Power Pinning Board shows where which components should be mounted:

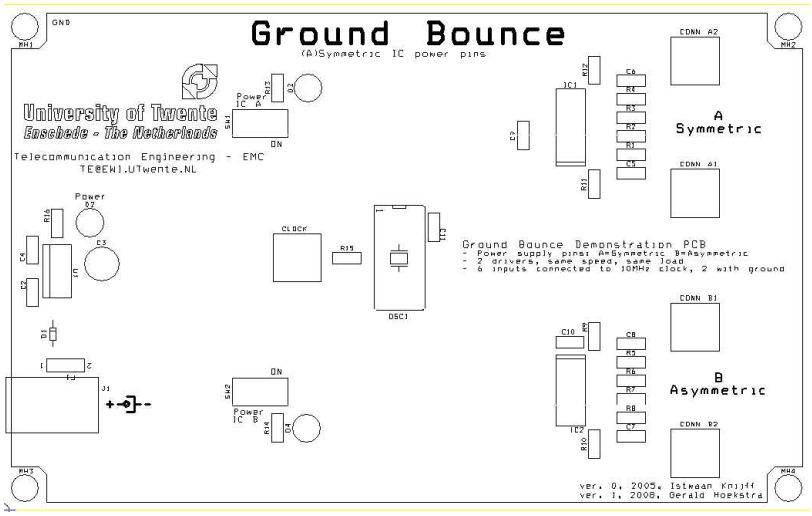

Figure 15.2: The Ground Bounce: Power Pinning Board Silk Screen.

15.2.3 Bare Board Top View

The etch pattern of the empty board, seen from the top side, is shown in Figure 15.3.

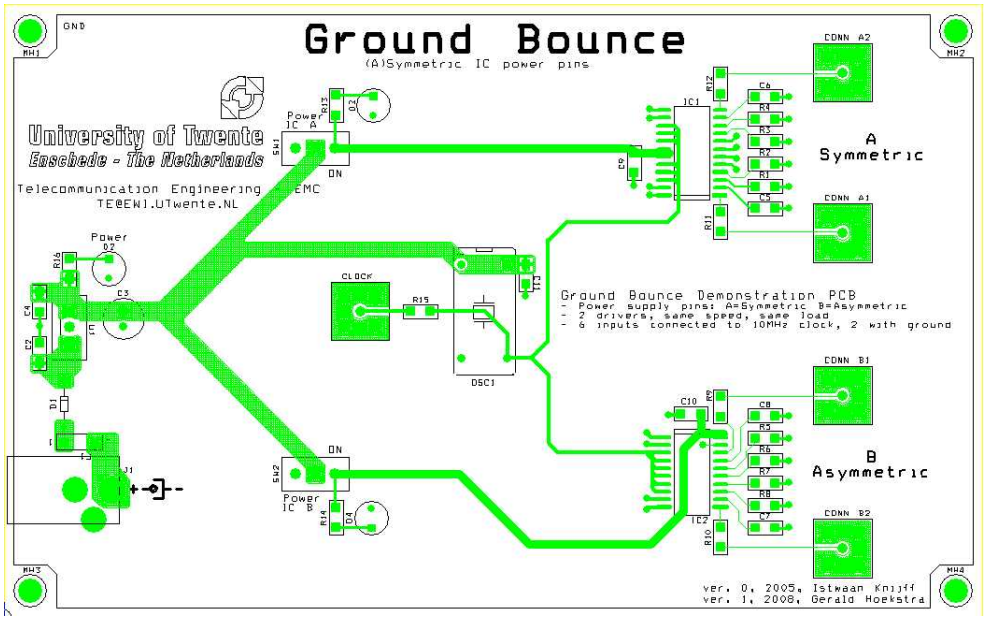

Figure 15.3: The Ground Bounce: Power Pinning Bare Board (Top View)

15.3 Bare Board Bottom View

The etch pattern of the empty board, seen from the bottom side, is shown in Figure 15.4.

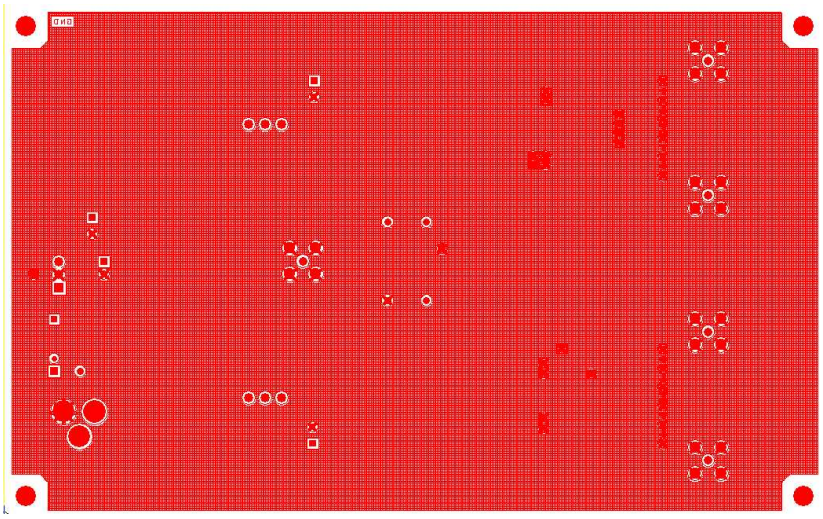

Figure 15.4: The Ground Bounce: Power Pinning Bare Board (Bottom View)

15.4 The Board Schematic

The schematic diagram of the Ground Bounce: Power Pinning Board is shown in Figure 15.5

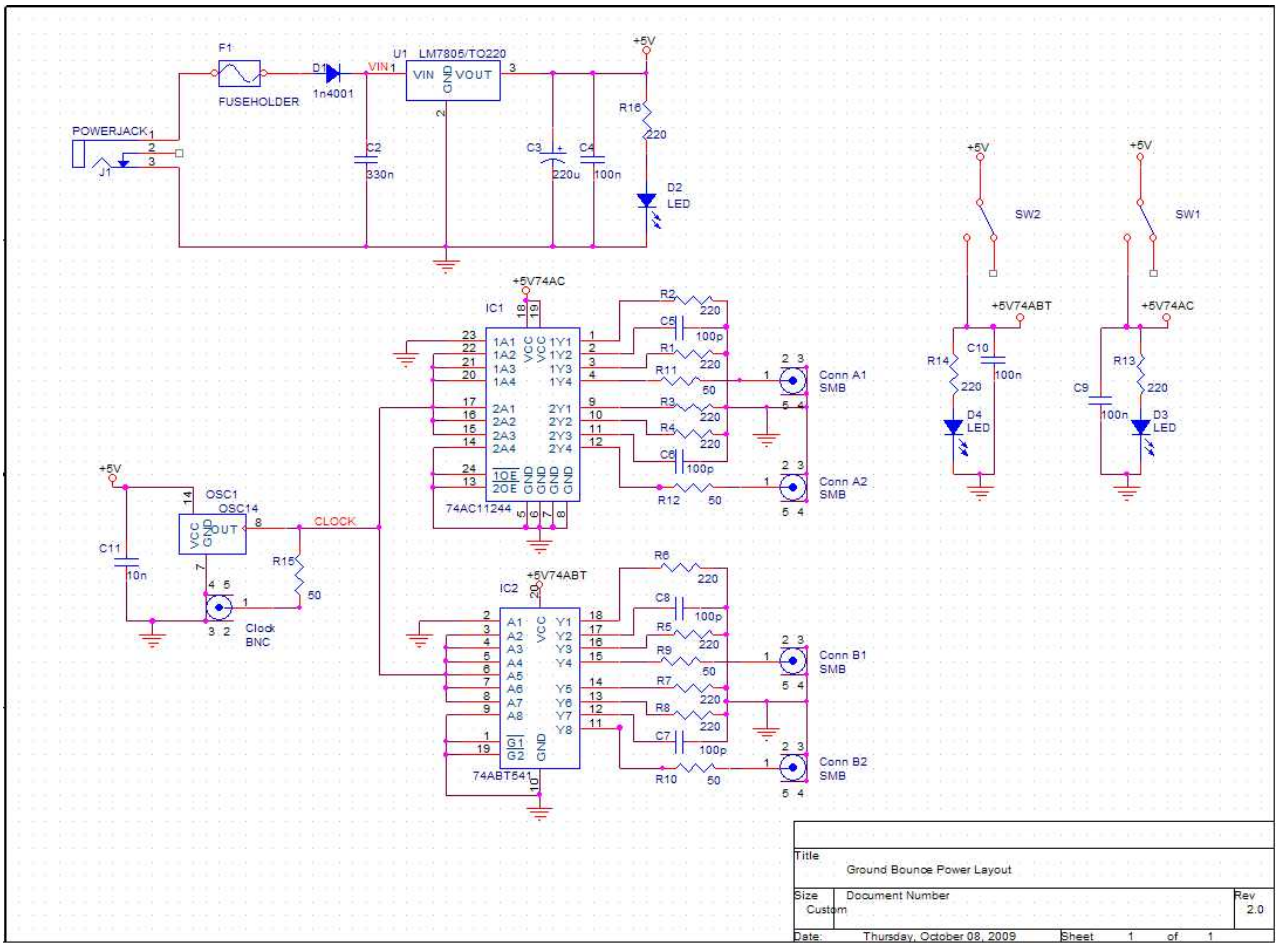

Figure 15.5: The Ground Bounce: Power Pinning Board Schematic.

15.5 The Bill of Materials

The components to complete the Ground Bounce: Power Pinning Board are shown in Table 15.1.

Table 15.1: Bill of Materials of the Ground Bounce: Power Pinning Board

REF DES	VALUE	PACKAGE	FOOTPRINT
C2	220n	CAP_NP	SM/C_1206
C3	100u	CAP_POL_0	CYL/D.275/LS.100/.034
C4	22n	CAP_NP	SM/C_1206
C5	100p	CAP_NP	SM/C_1206

Table 15.1: Bill of Materials of the Ground Bounce: Power Pinning Board (cont'd)

REF DES	VALUE	PACKAGE	FOOTPRINT
C7	100p	CAP_NP	SM/C_1206
C8	100p	CAP_NP	SM/C_1206
C9	100n	CAP_NP	SM/C_1206
C10	100n	CAP_NP	SM/C_1206
C11	10n	CAP_NP	SM/C_1206
CLOCK	SMB	SMB	RF/SMB/V
CONN A1	SMB	SMB	RF/SMB/V
CONN A2	SMB	SMB	RF/SMB/V
CONN B1	SMB	SMB	RF/SMB/V
CONN B2	SMB	SMB	RF/SMB/V
D1	1n4001	DIODE_0	DAX2/1N_4001-4007_REV1
D2	LED RED	LED	CYL/D.225/LS.125/.031
D3	LED YEL	LED	CYL/D.225/LS.125/.031
D4	LED GRN	LED	CYL/D.225/LS.125/.031
F1	FUSEHOLDER	FUSEHOLDER	BLKCON.200/VH/TM1SQ/W.100/2
IC1	74AC11244	74AC11244	SOG.050/24/WG.420/L.600
IC2	74ABT541	74ABT541_0	SOG.050/20/WG.420/L.500
J1	CONN PWR 2-J	PHONEJACK_0	POWERJACK
OSC1	10 MHz	OSC14	OSC
R1	220	RESISTOR	SM/R_1206
R2	220	RESISTOR	SM/R_1206
R3	220	RESISTOR	SM/R_1206
R4	220	RESISTOR	SM/R_1206
R5	220	RESISTOR	SM/R_1206
R6	220	RESISTOR	SM/R_1206
R7	220	RESISTOR	SM/R_1206
R8	220	RESISTOR	SM/R_1206
R9	50	RESISTOR	SM/R_1206
R10	50	RESISTOR	SM/R_1206
R11	50	RESISTOR	SM/R_1206
R12	50	RESISTOR	SM/R_1206
R13	220	RESISTOR	SM/R_1206
R14	220	RESISTOR	SM/R_1206
R15	50	RESISTOR	SM/R_1206
R16	220	RESISTOR	SM/R_1206
SW1	SW KEY-SPDT	SW_KEY-SPDT_1	SLIDESWITCH
SW2	SW KEY-SPDT	SW_KEY-SPDT_1	SLIDESWITCH
U1	L7805/TO220	L7805/TO220_2	TO220AA/RF1

15.6 Board Functional Description

The “Ground Bounce: Power Pinning” Board is built up as the “Ground Bounce: Package Type” board described in chapter 13. The differences are:

- Only two IC’s are available as “test objects”.
- The IC’s are functionally (for our purpose here) identical octal drivers but for the Power pins.
- The IC 74AC11244 has, so called, “center pinning”. Power is provided through the pins in the middle of the package.
- The IC 74ABT541 has the traditional “end pinning” where power is provided via pins diagonally opposite to each other.

The idea is that the center pinning type has less bonding wire inductance and hence should show less “Ground Bounce”. This is augmented by the fact that the 74AC11244 chip has two parallel V_{CC} and four “GND” pins. This should reduce the GND bonding inductance by a factor of 4. The connection to power supply and oscilloscope and switching on and off the two tested IC sections is described in chapter 13, Section 13.3. The measured results, the clock and Ground Bounce signals of the two IC’s are shown in Figure 15.6.

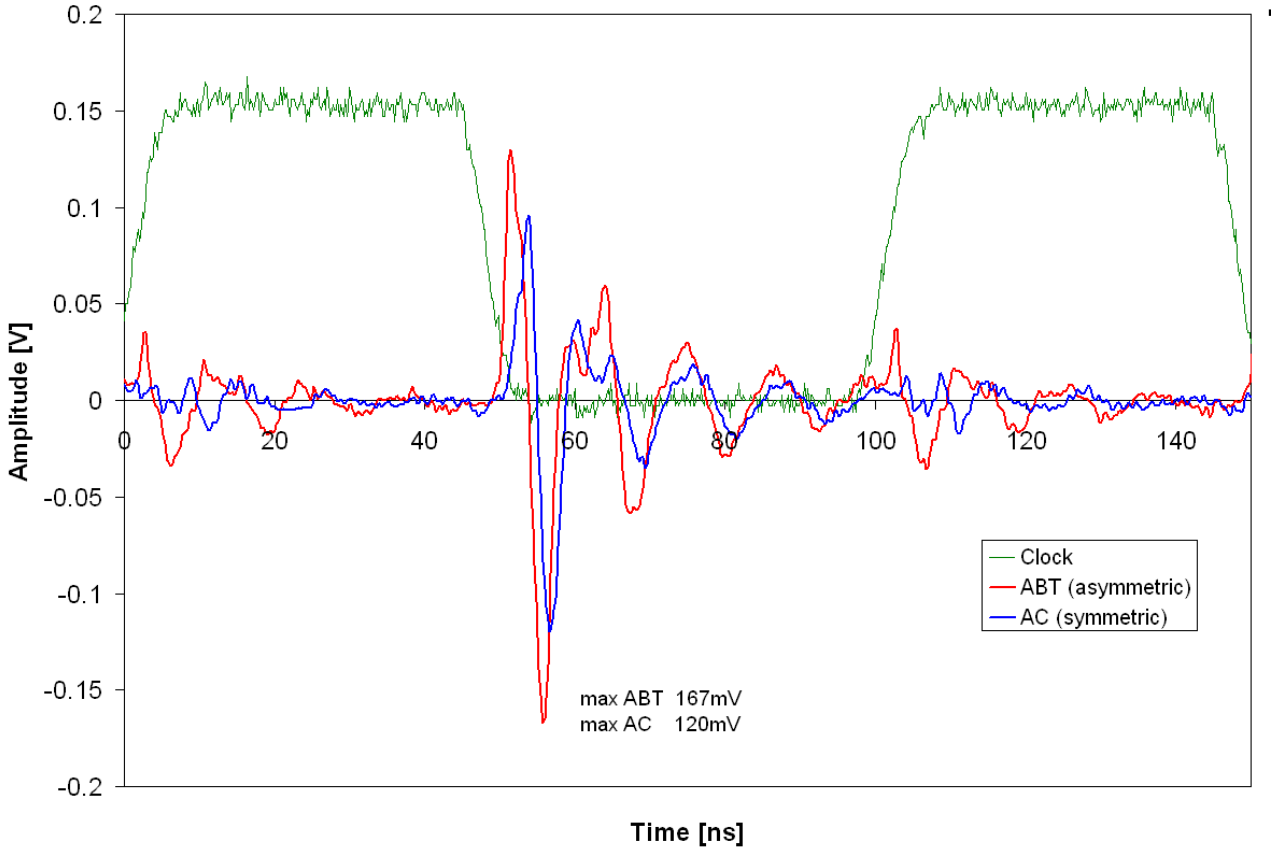

Figure 15.6: Ground Bounce Spikes Measured on both IC’s Outputs

15.7 Lessons Learned

The “Ground Bounce: Power Pinning” experiments show that:

1. The ground bounce from the center pinned chip is slightly lower than that of the end pinning type. But not a factor of 4 less.
2. Other factors like the placement and wiring of the decoupling capacitor and ground traces and via’s are equally important.

Chapter 16

Ground Bounce: Power Pinning Mk2

Contents

16.1 Demonstrations on the Ground Bounce: Power Pinning Mk2 Board

The Ground Bounce: Power Pinning Board Mk2 shows the same effect as the Ground Bounce Package Type Mk2 Board but focusses on the difference between devices with end and center power pinning layout. Mk2 has an additional ground plane on the component side of the board to try to further reduce Ground Bounce.

16.2 Ground Bounce: Power Pinning Board Mk2 Views

16.2.1 The Finished Board

The end result of the assembly of the Ground Bounce: Power Pinning Mk2 Board is shown in Figure 16.1

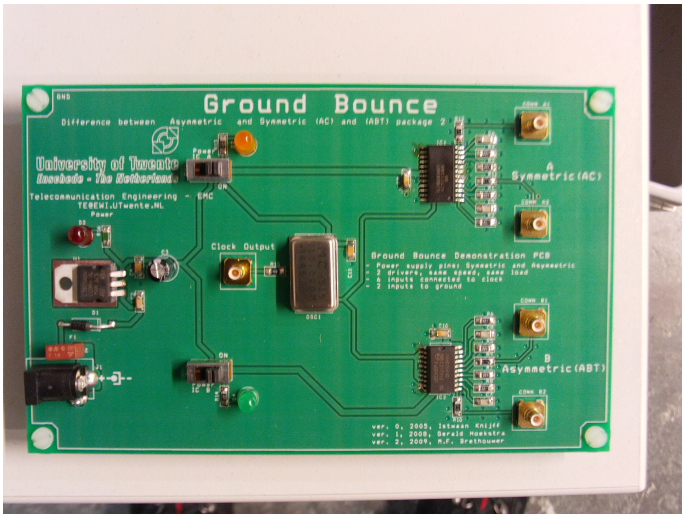

Figure 16.1: The Finished Ground Bounce: Power Pinning Board.

16.2.2 The Silkscreen

The Silkscreen of the Ground Bounce: Power Pinning Mk2 Board shows where which components should be mounted:

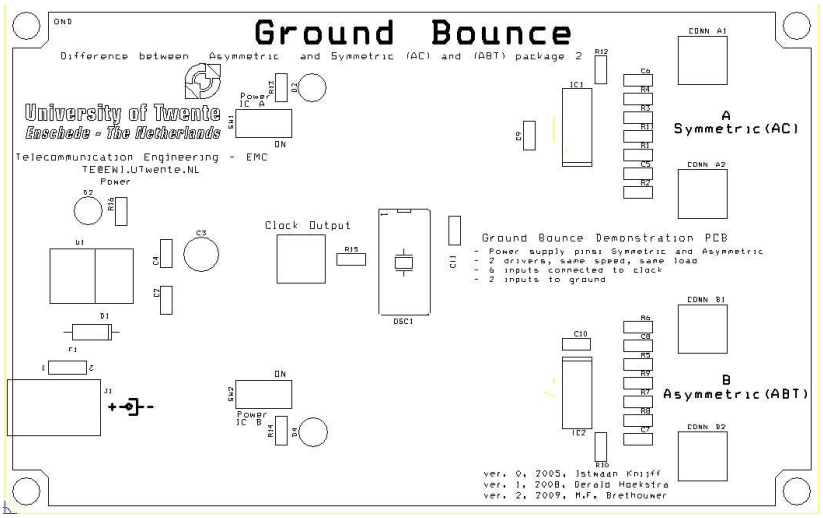

Figure 16.2: The Ground Bounce: Power Pinning Mk2 Board Silk Screen.

16.2.3 Bare Board Top View

The etch pattern of the empty board, seen from the top side, is shown in Figure 16.3.

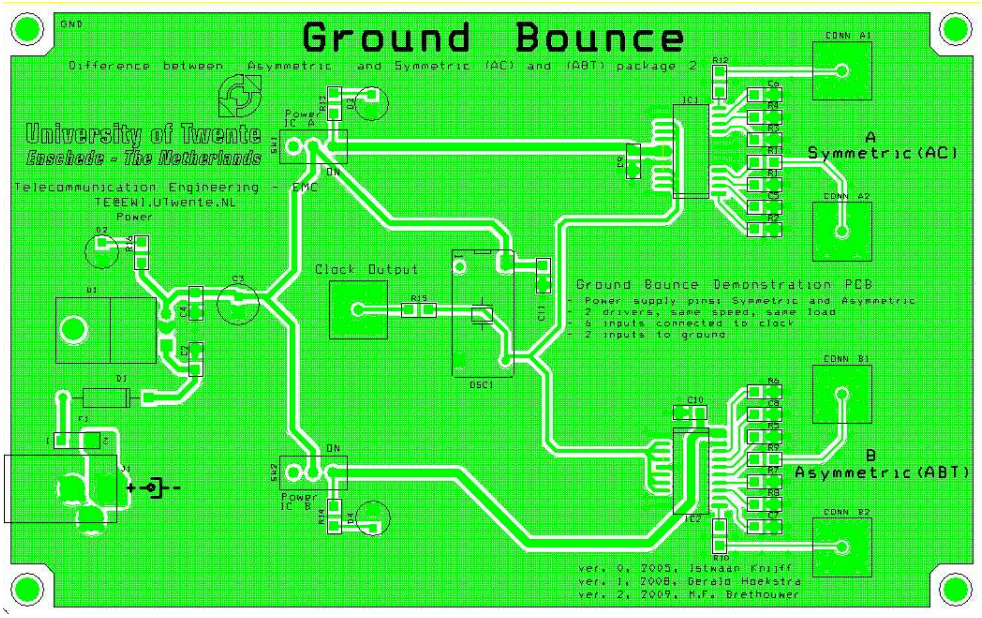

Figure 16.3: The Ground Bounce: Power Pinning Mk2 Bare Board (Top View)

16.3 Bare Board Bottom View

The etch pattern of the empty Mk2 board, seen from the bottom side, is shown in Figure 16.4.

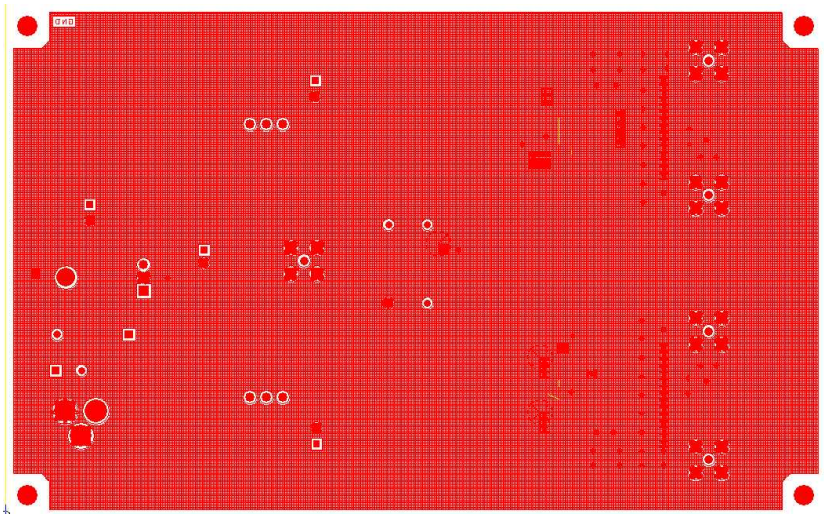

Figure 16.4: The Ground Bounce: Power Pinning Mk2 Bare Board (Bottom View)

16.4 The Board Schematic

The schematic diagram of the Ground Bounce: Power Pinning Board is shown in Figure 16.5

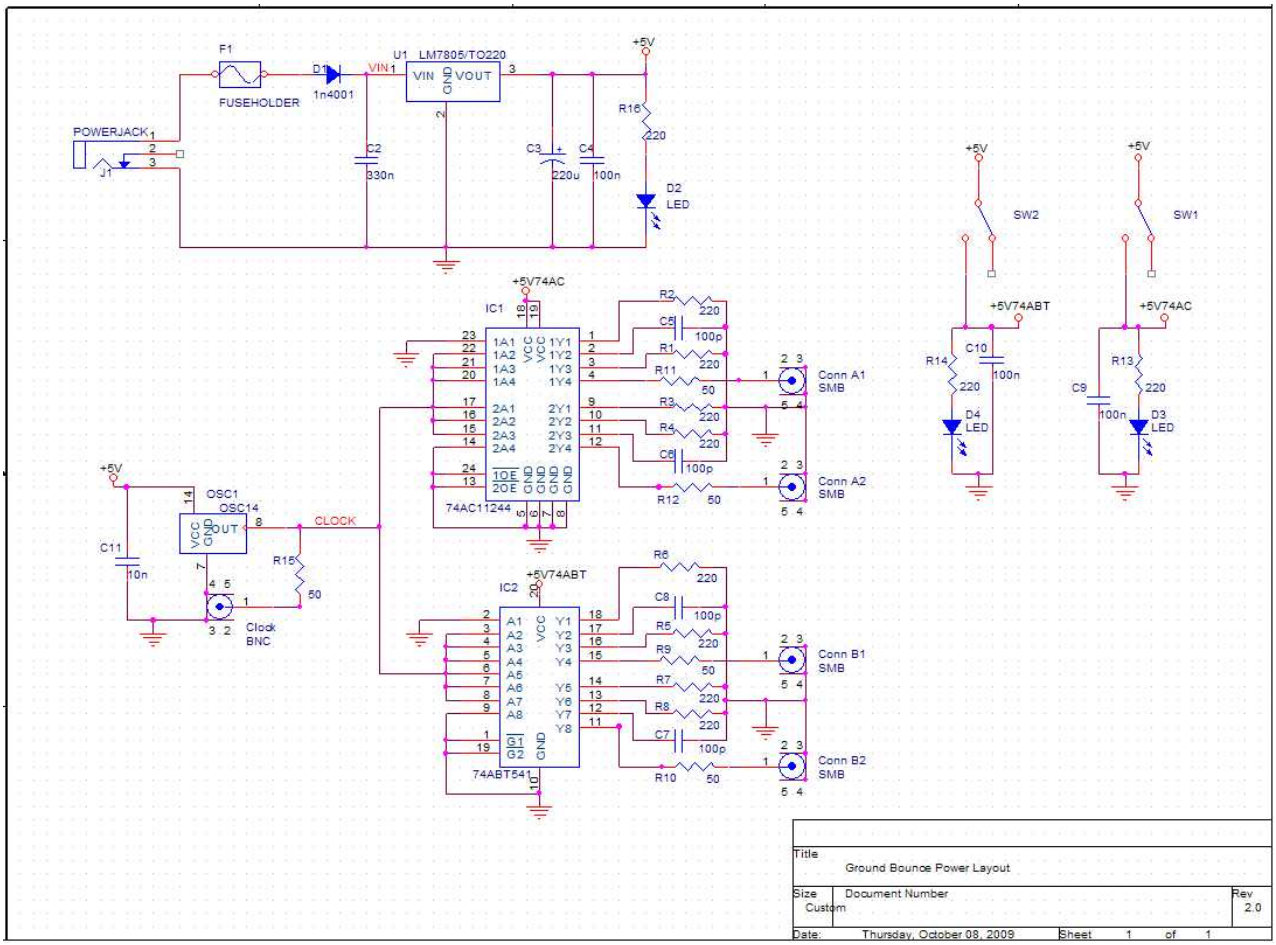

Figure 16.5: The Ground Bounce: Power Pinning Mk2 Board Schematic.

16.5 The Bill of Materials

The components to complete the Ground Bounce: Power Pinning Mk2 Board are shown in Table 16.1.

Table 16.1: Bill of Materials of the Ground Bounce: Power Pinning Mk2 Board

REF DES	VALUE	PACKAGE	FOOTPRINT
C2	220n	CAP_NP	SM/C_1206
C3	100u	CAP_POL_0	CYL/D.275/LS.100/.034
C4	22n	CAP_NP	SM/C_1206

Table 16.1: Bill of Materials of the Ground Bounce: Power Pinning Mk2 Board (cont'd)

REF DES	VALUE	PACKAGE	FOOTPRINT
C5	100p	CAP_NP	SM/C_1206
C7	100p	CAP_NP	SM/C_1206
C8	100p	CAP_NP	SM/C_1206
C9	100n	CAP_NP	SM/C_1206
C10	100n	CAP_NP	SM/C_1206
C11	10n	CAP_NP	SM/C_1206
CLOCK	SMB	SMB	RF/SMB/V
CONN A1	SMB	SMB	RF/SMB/V
CONN A2	SMB	SMB	RF/SMB/V
CONN B1	SMB	SMB	RF/SMB/V
CONN B2	SMB	SMB	RF/SMB/V
D1	1n4001	DIODE_0	DAX2/1N_4001-4007_REV1
D2	LED RED	LED	CYL/D.225/LS.125/.031
D3	LED YEL	LED	CYL/D.225/LS.125/.031
D4	LED GRN	LED	CYL/D.225/LS.125/.031
F1	FUSEHOLDER	FUSEHOLDER	BLKCON.200/VH/TM1SQ/W.100/2
IC1	74AC11244	74AC11244	SOG.050/24/WG.420/L.600
IC2	74ABT541	74ABT541_0	SOG.050/20/WG.420/L.500
J1	CONN PWR 2-J	POWERJACK_0	POWERJACK
OSC1	10 MHz	OSC14	OSC
R1	220	RESISTOR	SM/R_1206
R2	220	RESISTOR	SM/R_1206
R3	220	RESISTOR	SM/R_1206
R4	220	RESISTOR	SM/R_1206
R5	220	RESISTOR	SM/R_1206
R6	220	RESISTOR	SM/R_1206
R7	220	RESISTOR	SM/R_1206
R8	220	RESISTOR	SM/R_1206
R9	50	RESISTOR	SM/R_1206
R10	50	RESISTOR	SM/R_1206
R11	50	RESISTOR	SM/R_1206
R12	50	RESISTOR	SM/R_1206
R13	220	RESISTOR	SM/R_1206
R14	220	RESISTOR	SM/R_1206
R15	50	RESISTOR	SM/R_1206
R16	220	RESISTOR	SM/R_1206
SW1	SW KEY-SPDT	SW_KEY-SPDT_1	SLIDESWITCH
SW2	SW KEY-SPDT	SW_KEY-SPDT_1	SLIDESWITCH
U1	L7805/TO220	L7805/TO220_2	TO220AA/RF1

16.6 Board Functional Description

The “Ground Bounce: Power Pinning” Board is built up as the “Ground Bounce: Package Type Mk2” board described in chapter 14. The differences are:

- Only two IC’s are available as “test objects”.
- The IC’s are functionally (for our purpose here) identical octal drivers but for the Power pins.
- The IC 74AC11244 has, so called, “center pinning”. Power is provided through the pins in the middle of the package.
- The IC 74ABT541 has the traditional “end pinning” where power is provided via pins diagonally opposite to each other.

The idea is that the center pinning type has less bonding wire inductance and hence should show less “Ground Bounce”. This is augmented by the fact that the 74AC11244 chip has two parallel V_{CC} and four “GND” pins. This should reduce the GND bonding inductance by a factor of 4. The connection to power supply and oscilloscope and switching on and off the two tested IC sections is as described in chapter 13, Section 13.3. The measured results, the Clock and Ground Bounce signals of the two IC’s are shown in Figure 16.6. Additionally, Figure 16.7 shows the Ground Bounce signals without the clock.

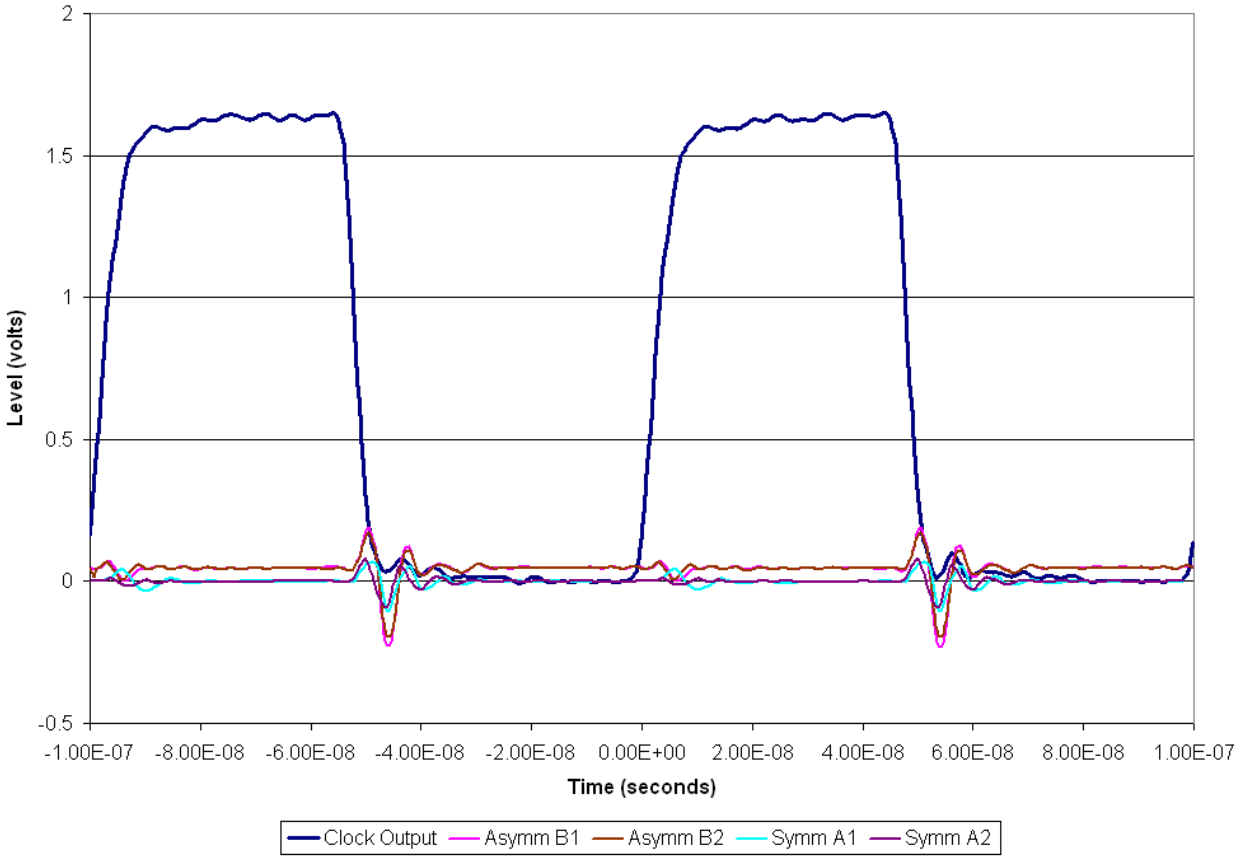

Figure 16.6: Clock and Ground Bounce Spikes Measured on both IC’s Outputs (Mk2 version)

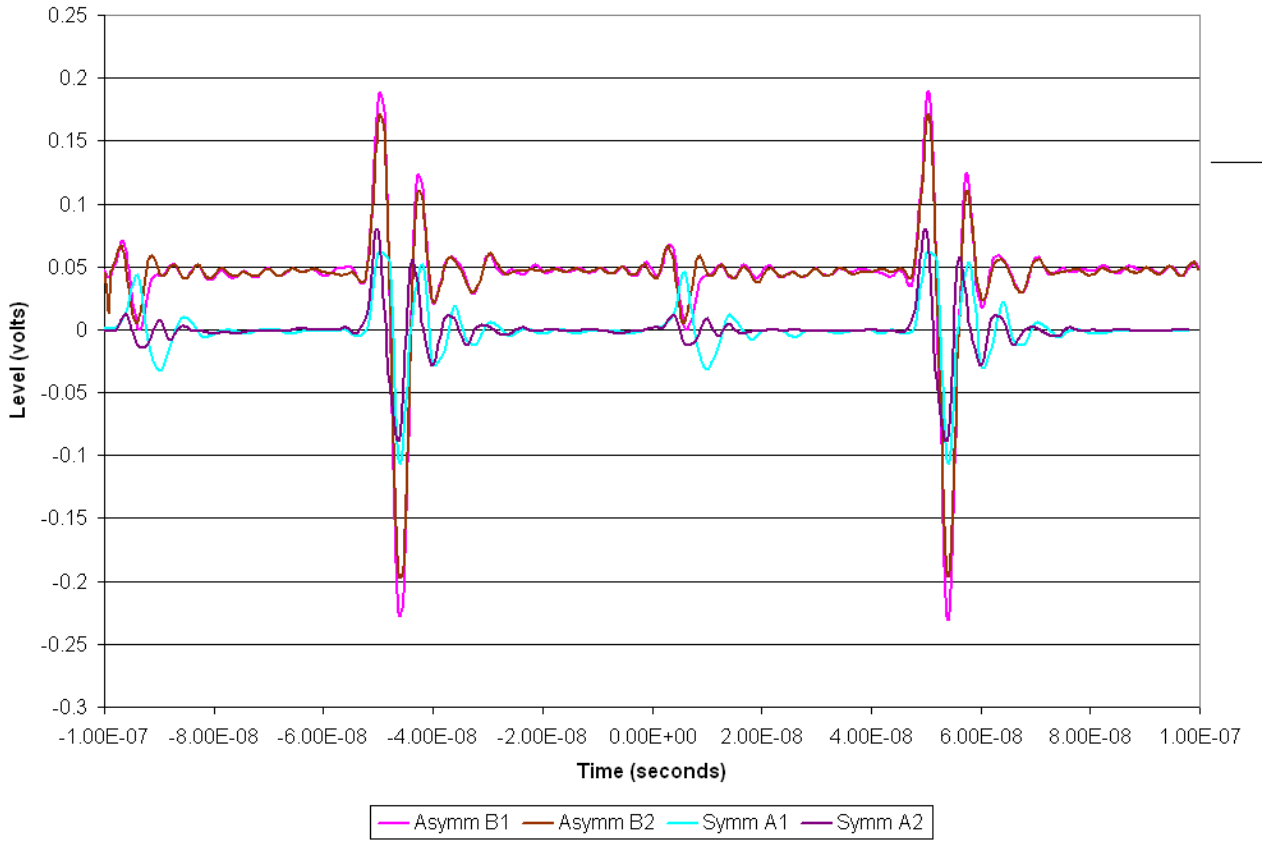

Figure 16.7: Ground Bounce Spikes on both IC's Outputs (Mk2 version)

16.7 Lessons Learned

The “Ground Bounce: Power Pinning Mk2” experiments show that:

1. The ground bounce from the center pinned chip is slightly lower than that of the end pinning type. But not a factor of 4 less.
2. Other factors like the placement and wiring of the decoupling capacitor and ground traces and via’s are equally important.

   And, for this Mk2 board:

3. Addition of an extra ground plane on the component side can help make the board ground connections shorter and hence reduce their inductance. This considerably reduces ground-bounce.

Chapter 17

General Remarks

Contents

17.1 The Future of the PCB Demo Boards

14 demonstration boards have been conceived and built so far. This, however, is an ongoing project. As the need arises, new experiments are sure to come up. Also, experience with the current boards will probably show how improvements can be made. New ways of meeting EMC problems will hopefully flow from it.

17.2 How the boards are built

17.2.1 User Expertise Required

It is assumed that the user of these demonstration boards has a reasonable knowledge of EMC. The boards are primarily intended for educational purposes. But the educator might not be interested or able to assemble the PCB's.

17.2.2 Experimenter Case with Finished Boards, Cables and Power Supply

The first option therefore is to have the boards assembled and tested by the University of Twente. In that case, the necessary cables and a power supply for the active boards will also be delivered. Everything in a useful carrying case. Measuring equipment like an oscilloscope and a spectrum analyzer with tracking generator will have to be provided by the user.

17.2.3 Do it Yourself

The other option is to order empty PCB boards. In that case, the educator/builder has to acquire the necessary components to assemble the boards. One of the items not mentioned in the Bills of Materials are the mounting feet the boards will stand on. We used nylon bolts and nuts, M3 x 12 mm. Each board has four mounting holes on the corners where these bolts can be inserted. Another option is to used adhesive plastic feet.
A final note on the connectors used on the demonstrations: we use SMB connectors for quick handling, but SMA types also fit. So, if you like, you can use your own preference. Here too, measuring equipment like an oscilloscope and a spectrum analyzer with tracking generator will have to be provided by the user.

17.3 Known Issues

17.3.1 Push-button Switches

Some of the boards have push-button momentary switches. After the production of the boards it became apparent that the shape “SWITCH-4PIN-TYCO-FSM4JH” used on some of the boards has been placed 90 degrees rotated. When placed in the position it fits, the connection will always exist whether pushed or not. The solution is to mount the switch in the normal way but to cut two of the 4 leads diagonally opposite to each other. Affected boards are the “Crosstalk Layout Issues” board in chapter 6 and the “Discontinuities: Ground Apertures” board in chapter 12.

17.3.2 Filters

The filters used on the “Grounding of Filters” board in chapter 10 were not fixed when the board was laid out. We used Murata enclosure wall mountable types. SMD models could be used just as well. Some improvisation is needed when mounting the filters as solder resist may have to be removed at places to provide sufficient access to the ground plane for connection of the return path. The L-shaped metal bracket will also have to be fabricated from thin brass or copper plate to connect the third filter. Finally, the “Plumbers Delight” construction requires complete coverage of one end of the filter with adhesive copper tape. Here too, solder resist may have to be removed locally.

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