EMC Design Rule Checking – Past, Present, and Future

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EMC SOCIETY

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Outline

- Past
  - History of EMC
  - Purpose of design rules
  - EMC fundamentals
    - Current
    - Impedance
  - EMC design rules
  - Evolution of design practices
- Present
  - Rule checking choices
  - Required capabilities
  - Considerations
- Future
  - Computing paradigm shift
  - ASIC design rules
  - System-Level rules
- Summary

History of EMC

- 1900 – 1970
  - Observation of electromagnetic interference in radios, television, and other communications
    - Causes are motors, engines, radar, power distribution lines, etc.
    - Increase in interference with introduction of transistors, ICs, and computing devices
- 1960s
  - Military and aerospace limits imposed
- 1979
  - FCC law limiting radiated emissions
- 1980 - 1990s
  - Emissions limits for computers, peripherals adopted by CISPR
  - Many other countries adopt European Norm (EN) requirements

History of EMC

- As soon as there were limits to meet and sales were at risk…
  - Increased focus on EMC
  - Collection of "lessons learned"
  - Analytical formulae developed from theory
  - Numerical modeling of simplified structures
  - > Development of design rules

- Late 1990s
  - Emergence of automated rule-checking tools
    - IBM developed internal tool in 1992
  - Formation of Research Consortium at University of Missouri at Rolla (UMR)

Automated EMC Design Rule-Checking: Fantasy vs Reality

- Fantastic Goal: Tell me if my product going to pass EMI testing
- Challenges:
  - Cannot simulate entire system
  - How do we extrapolate from local effects to far-field performance?
  - Products have unique challenges
    - Size, weight
    - Airflow requirements
    - Cables/connectors
    - Materials
- Realistic Goal: Identify violations of design rules and rank them by severity
  - EMC engineer can fix most severe violations and minimize risk of failure without overdesigning product

Electrical vs Mechanical Design Rules

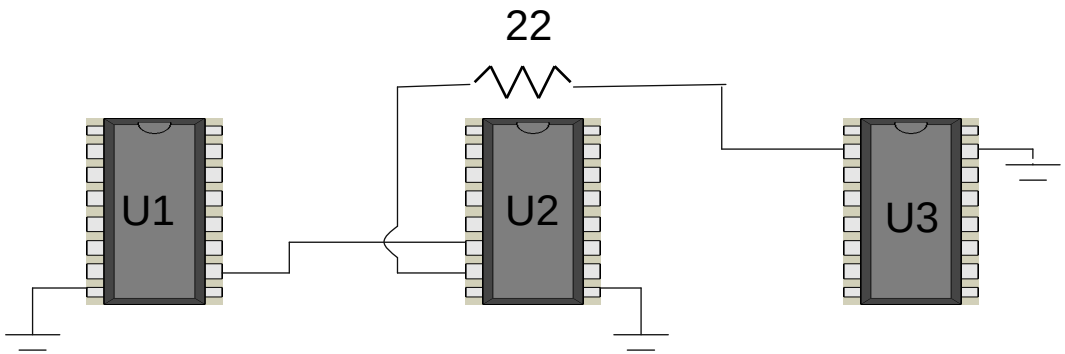
- Both electrical & mechanical designs are critical for overall system EMC performance
- Automation efforts have been limited to Electrical Rules
  - Circuit boards contain the sources of emissions and the victims of susceptibility
  - Circuit boards are more complex and more time consuming to review manually
    - True for simpler systems
    - Must be revisited for current systems
      - Complex high-performance computing racks
      - Modular, integrated products
  - Most EMC engineers have EE backgrounds

EM Wave Propagation

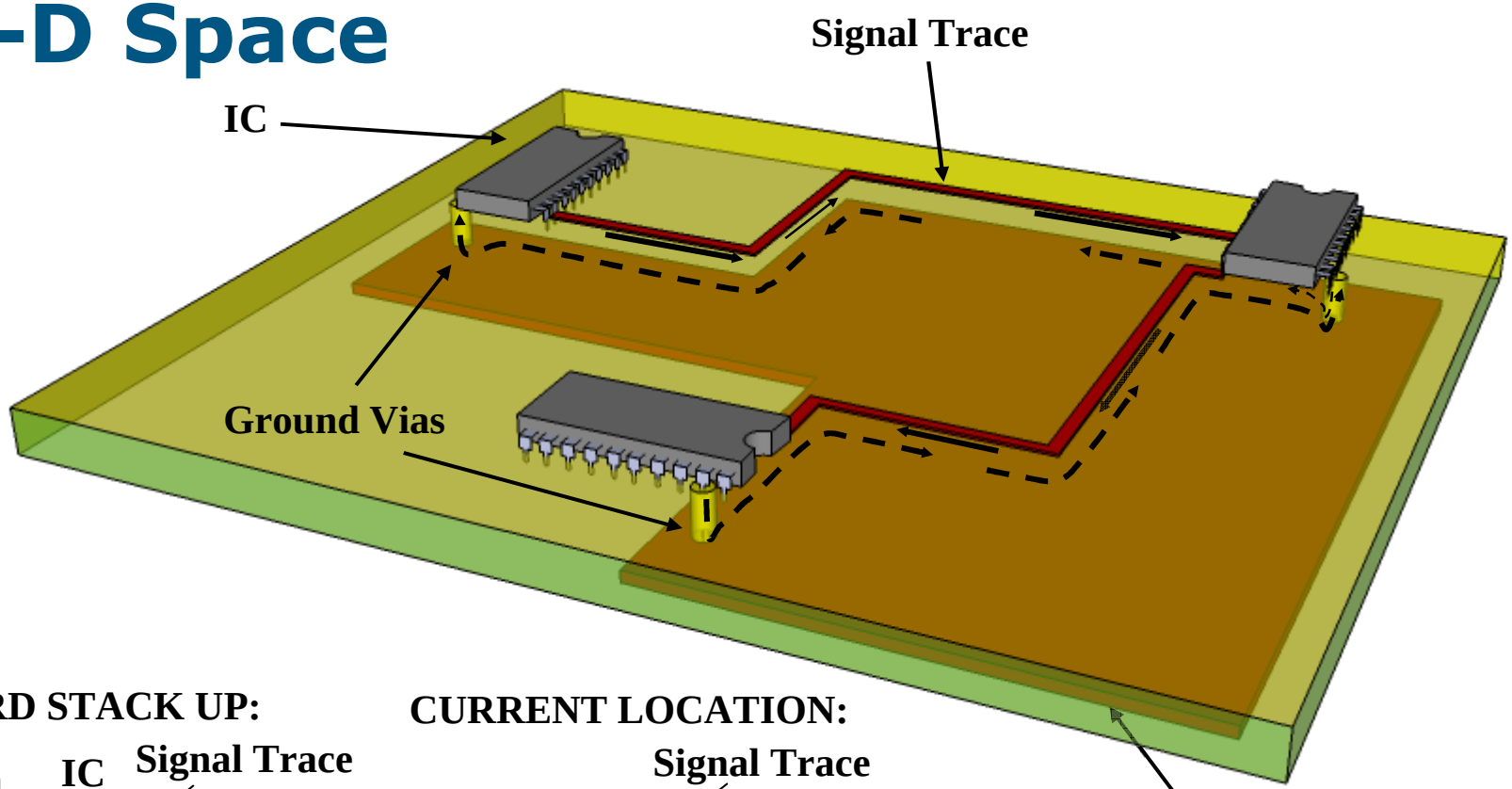
- Accelerating charge creates a propagating EM wave
  - Acceleration of charge = d^2Q/dt^2
  - I=dQ/dt, so a time-varying current (dI/dt) creates a propagating EM wave

- EMC is about currents

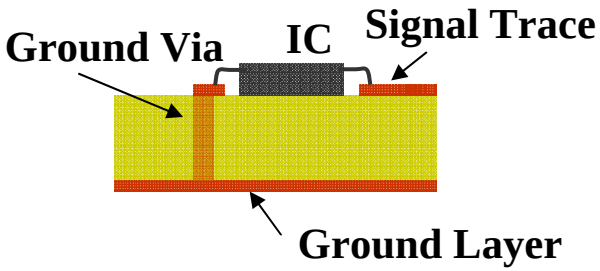
Can You Identify the EMC Problem from this Schematic?



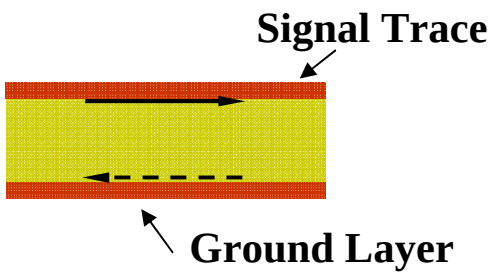
Follow the Entire Current Path in 3-D Space



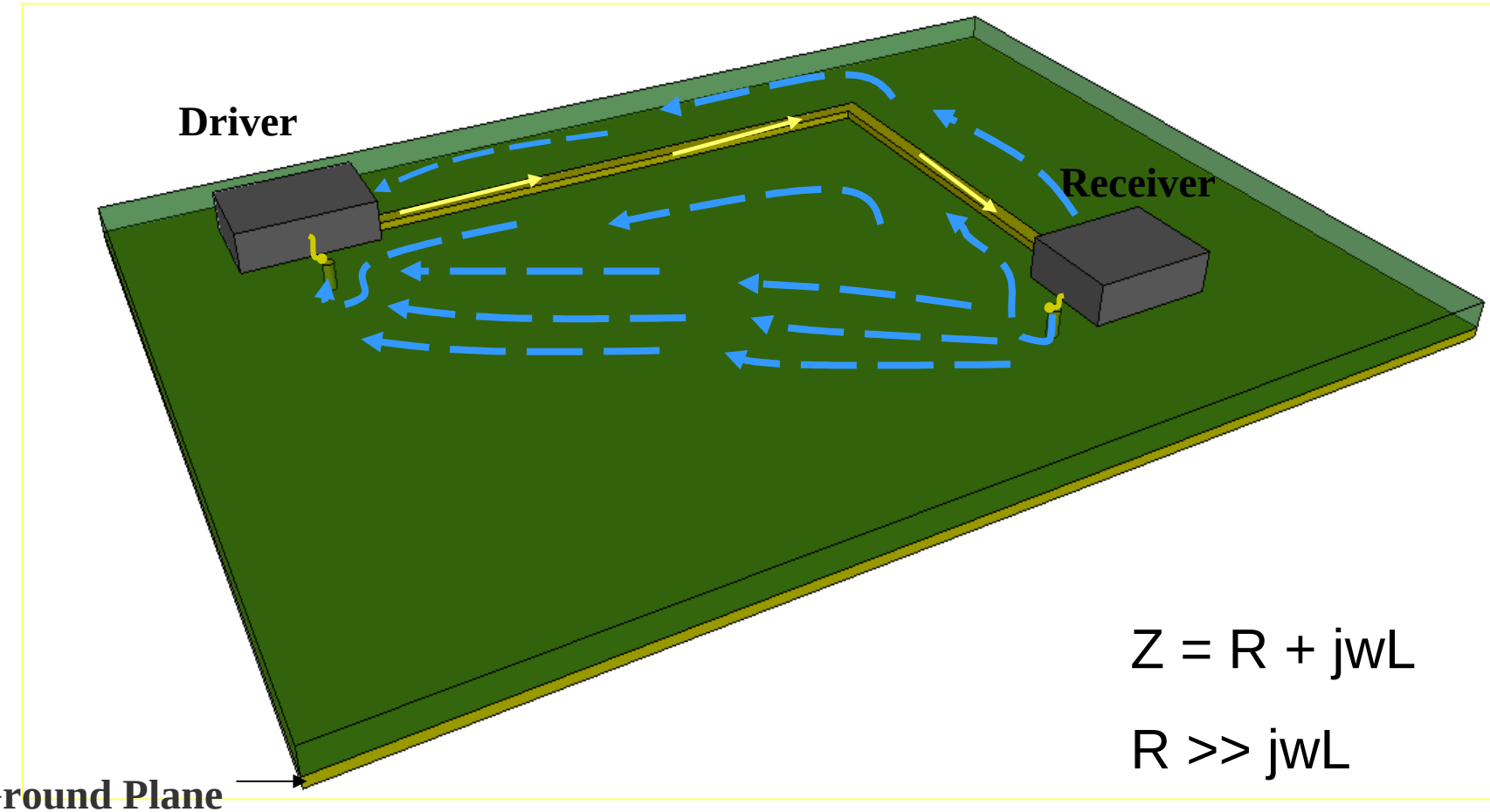
BOARD STACK UP:



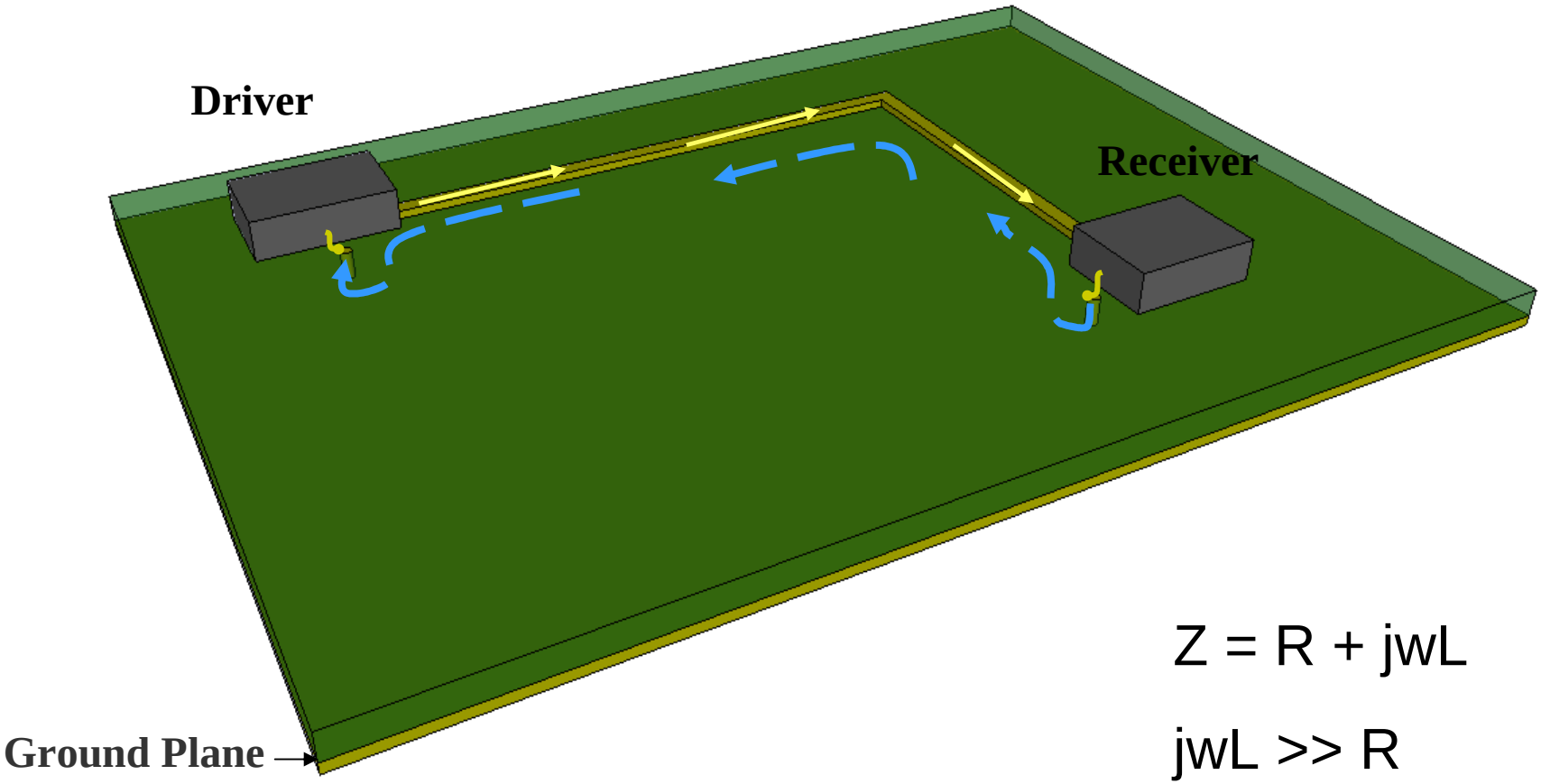
CURRENT LOCATION:



Low Frequency Return Currents Take Path of Least Resistance



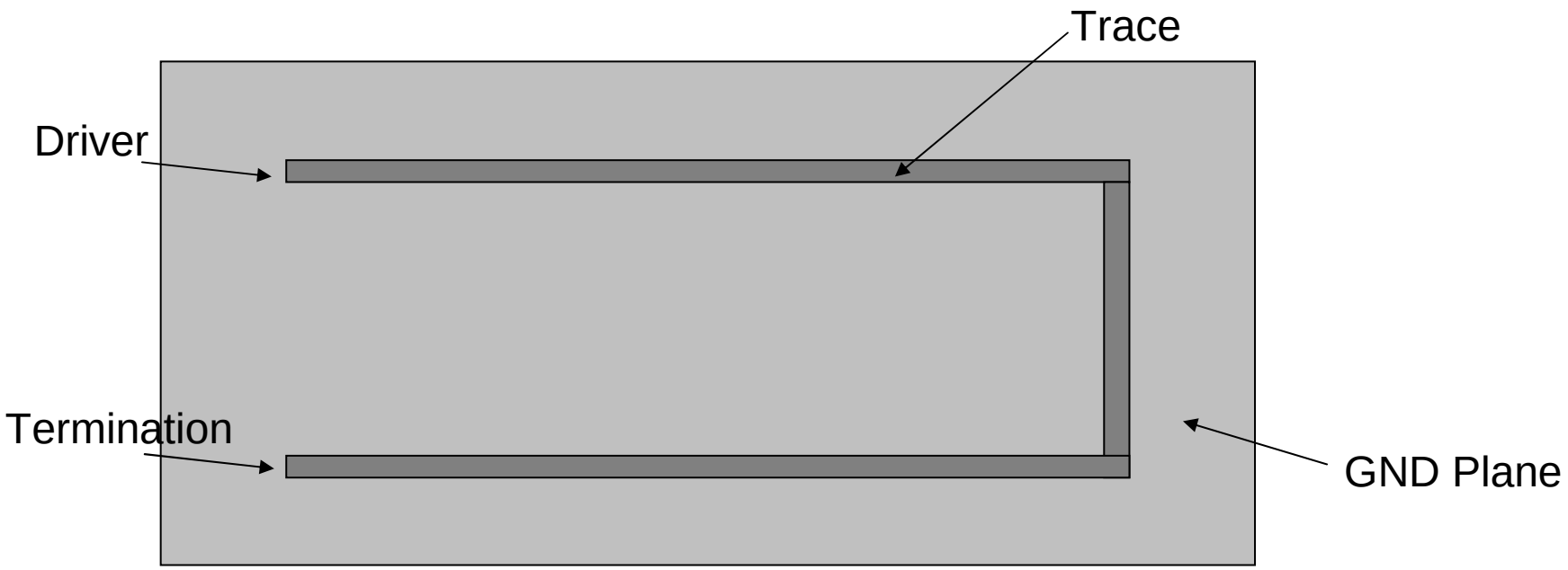
High Frequency Return Currents Take Path of Least Inductance



$$Z = R + jwL$$

$$jwL >> R$$

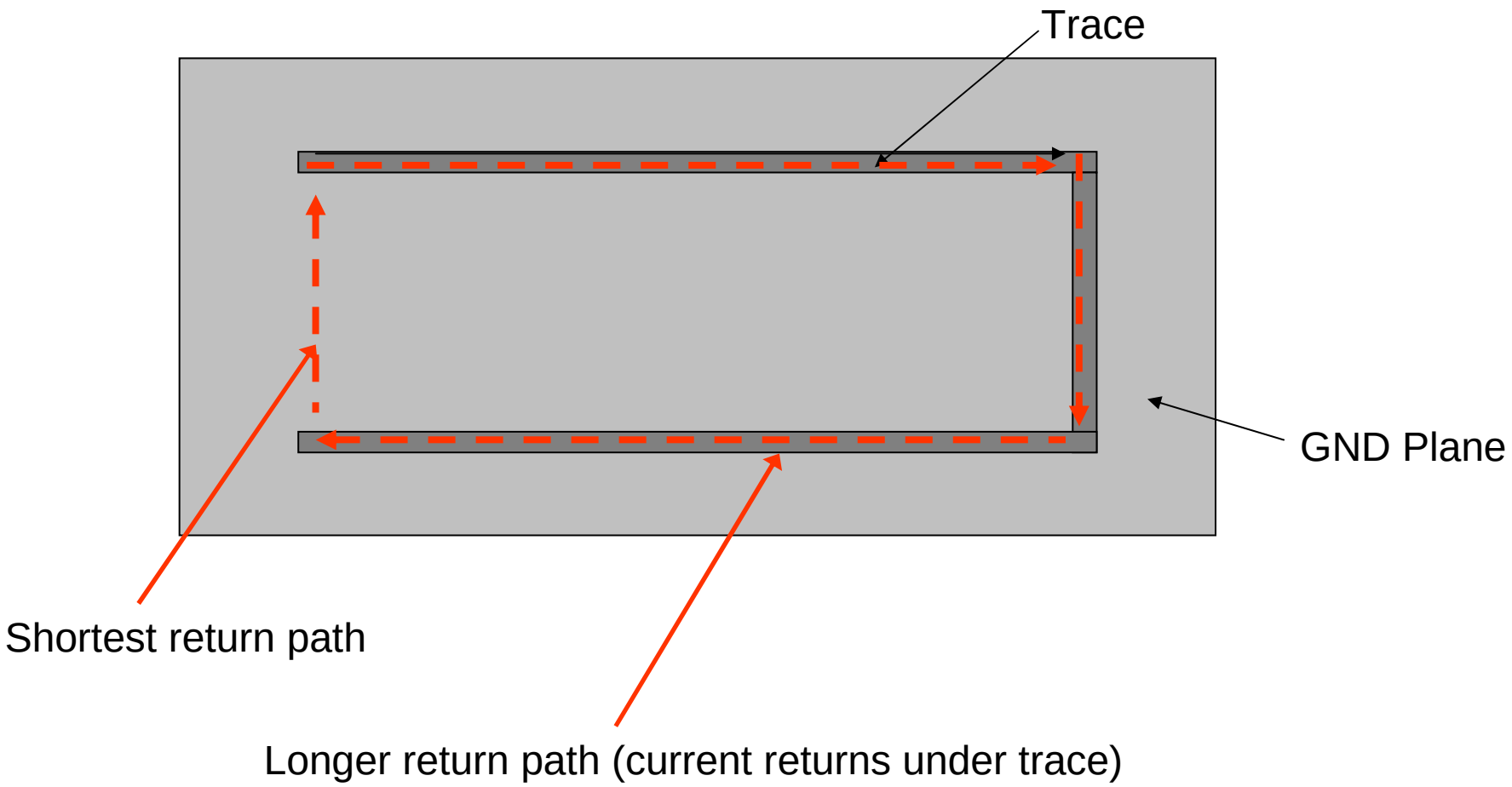
PCB Example for Return Current Impedance



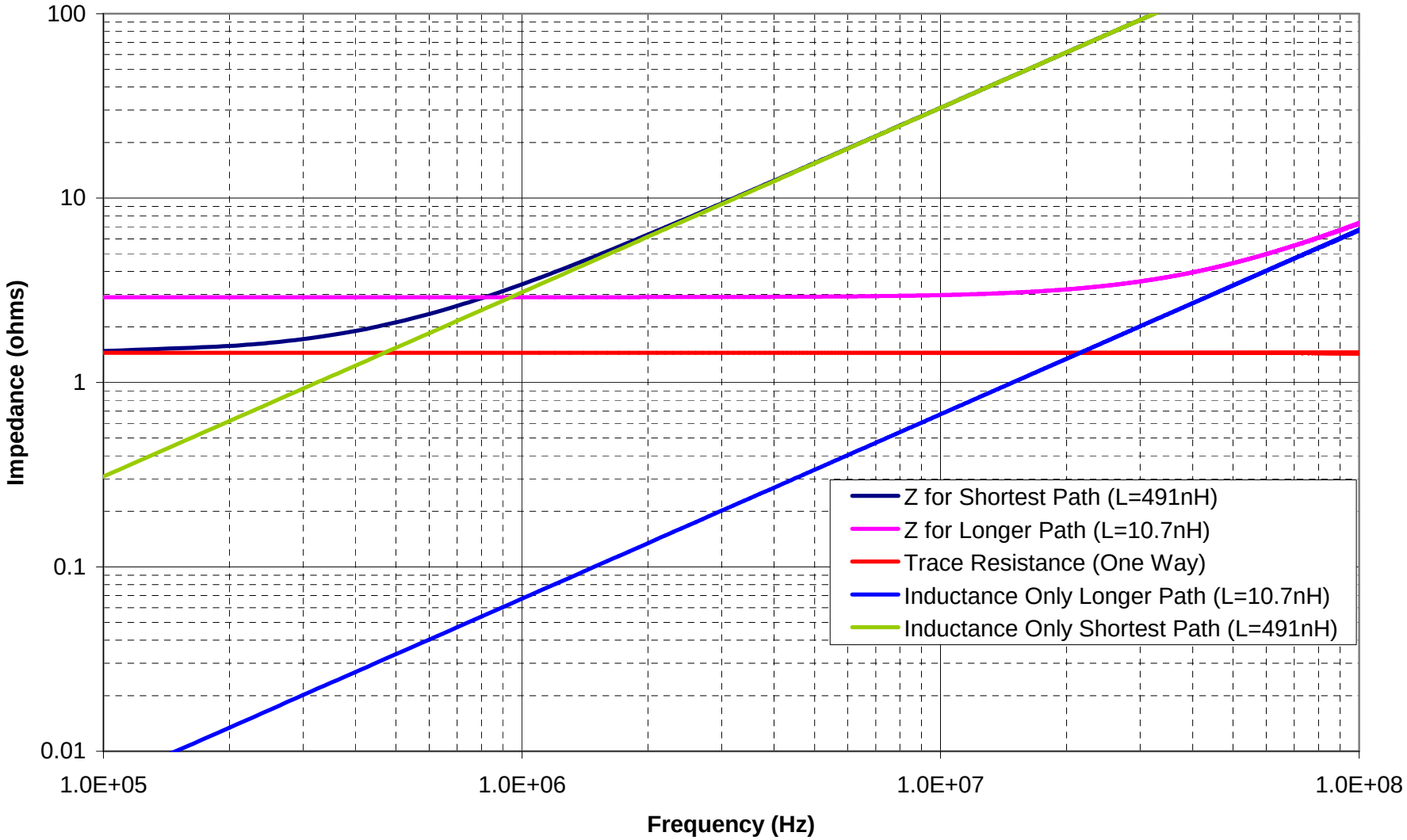
22” trace

10 mils wide, 1 mil thick, 10 mils above GND plane

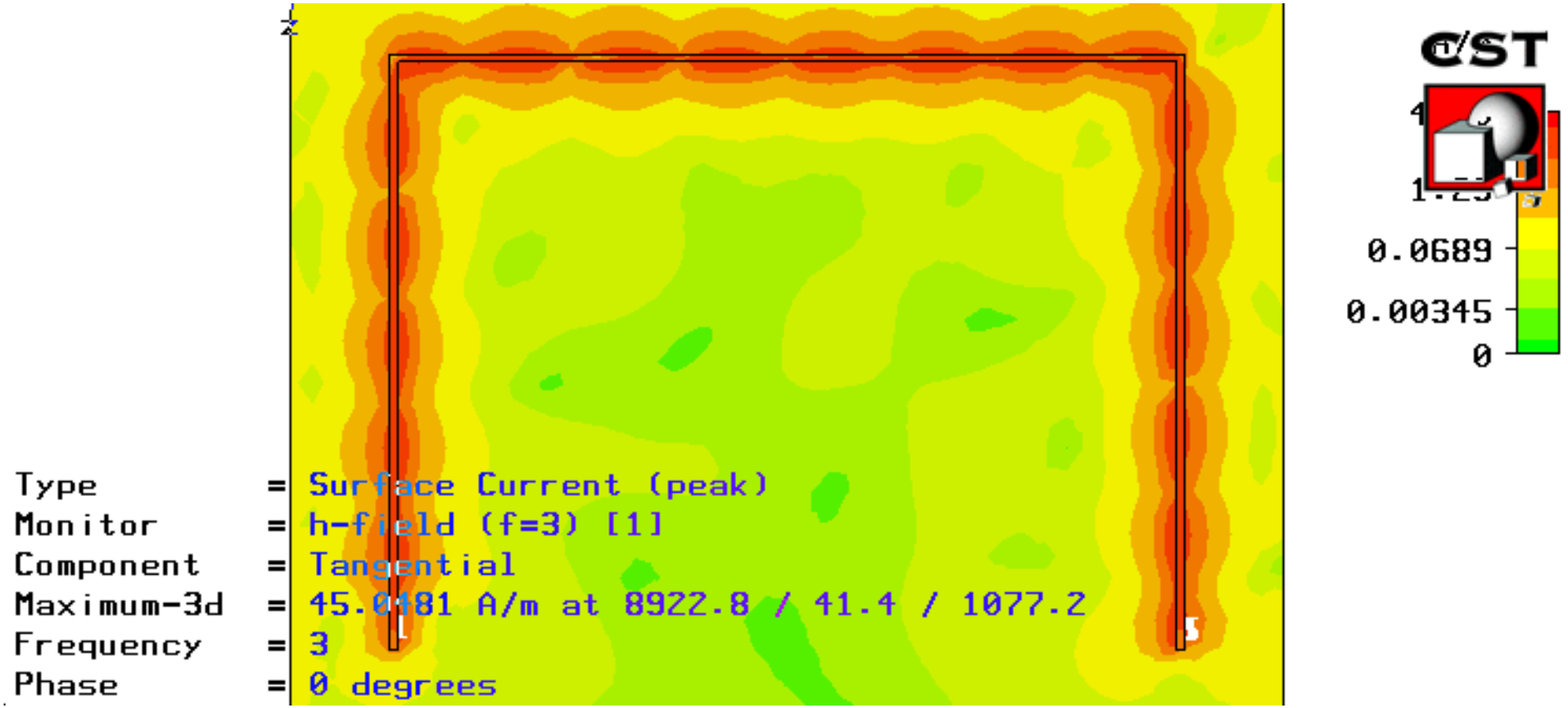
PCB Example for Return Current Impedance



Current Path Impedance Example for U-shaped 22" Trace



Surface Current Distribution/ Animation at High Frequency (3 GHz)



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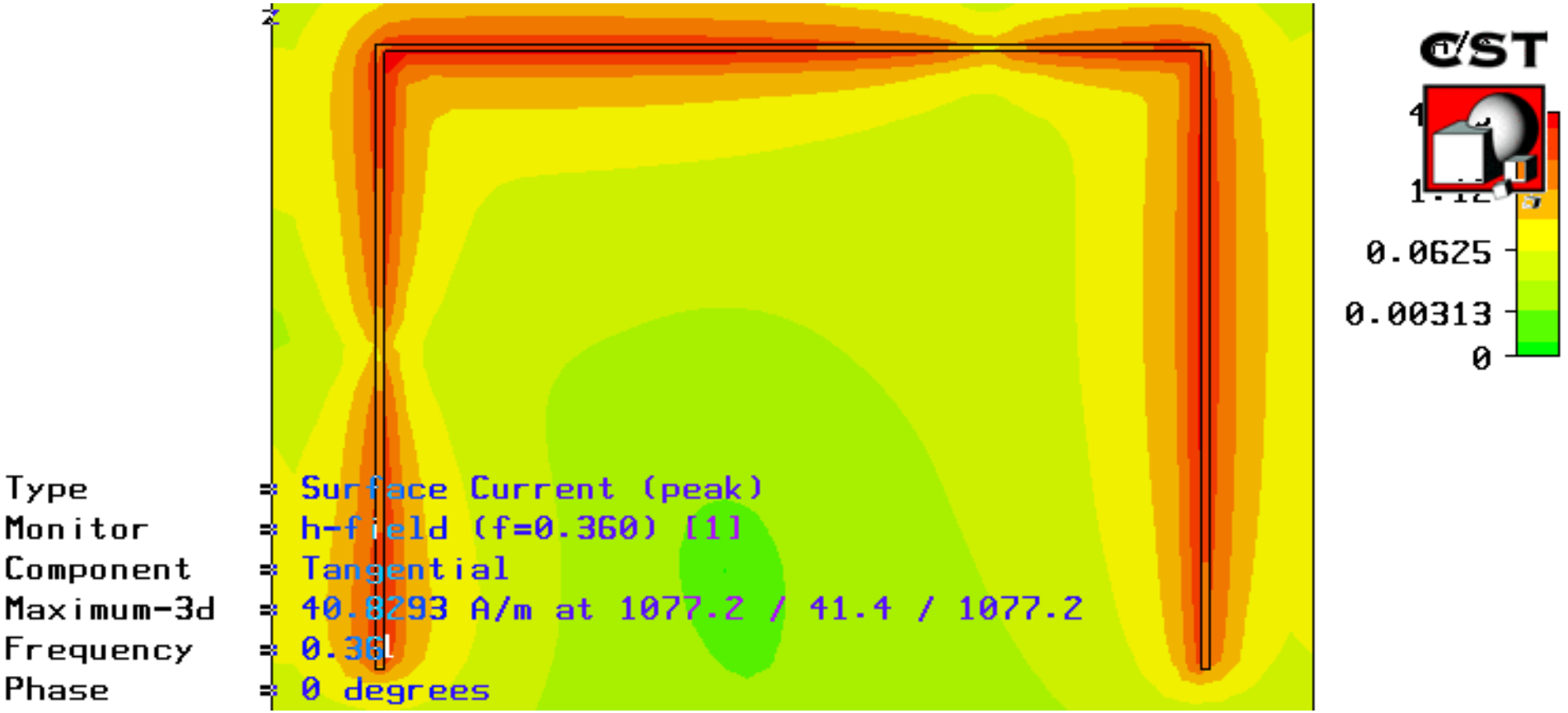
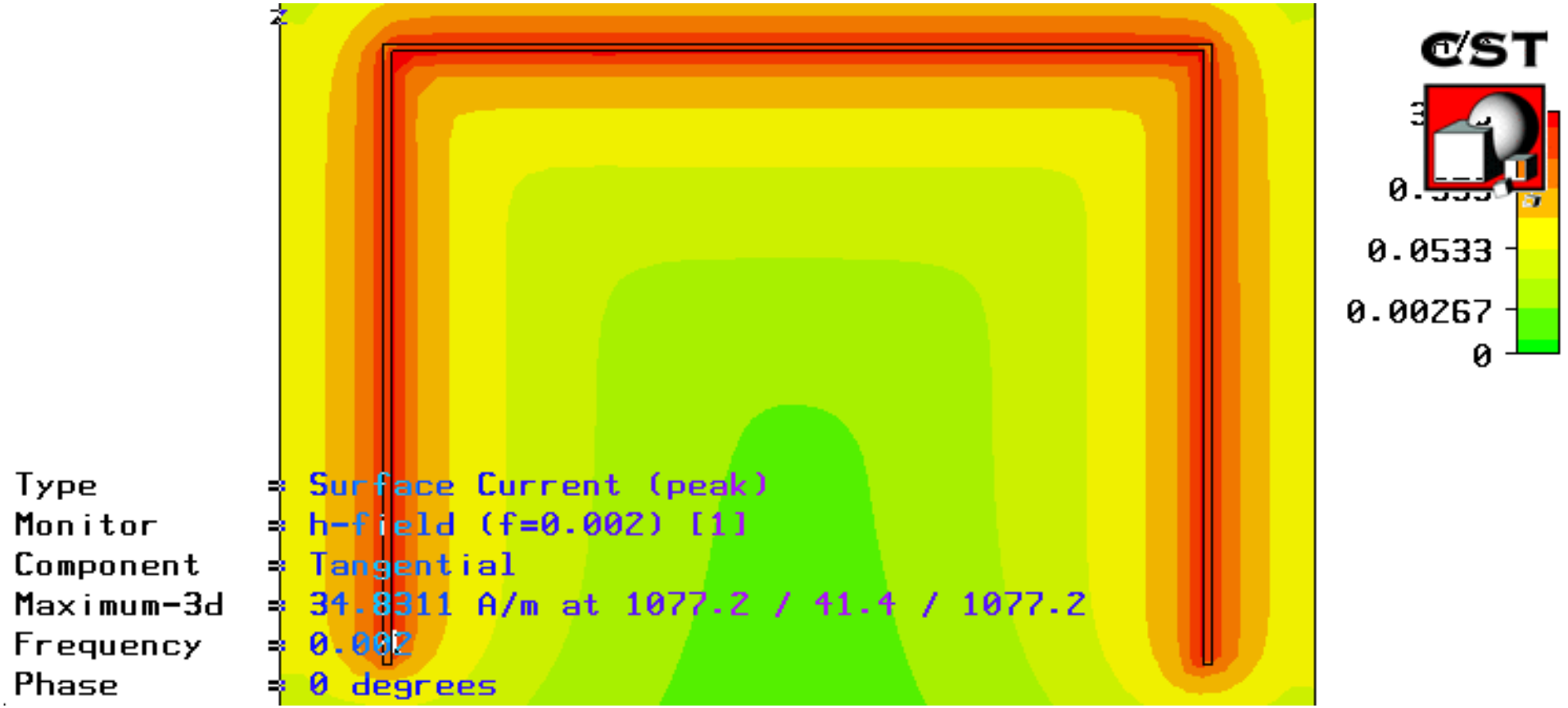
Surface Current Distribution/ Animation at Mid Frequency (360 MHz)



Surface Current Distribution/ Animation at Low Frequency (2 MHz)



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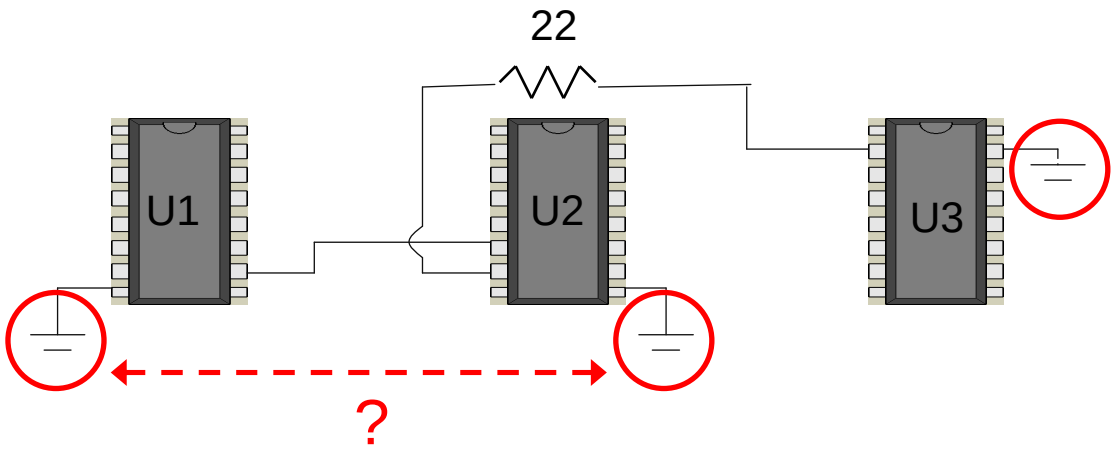
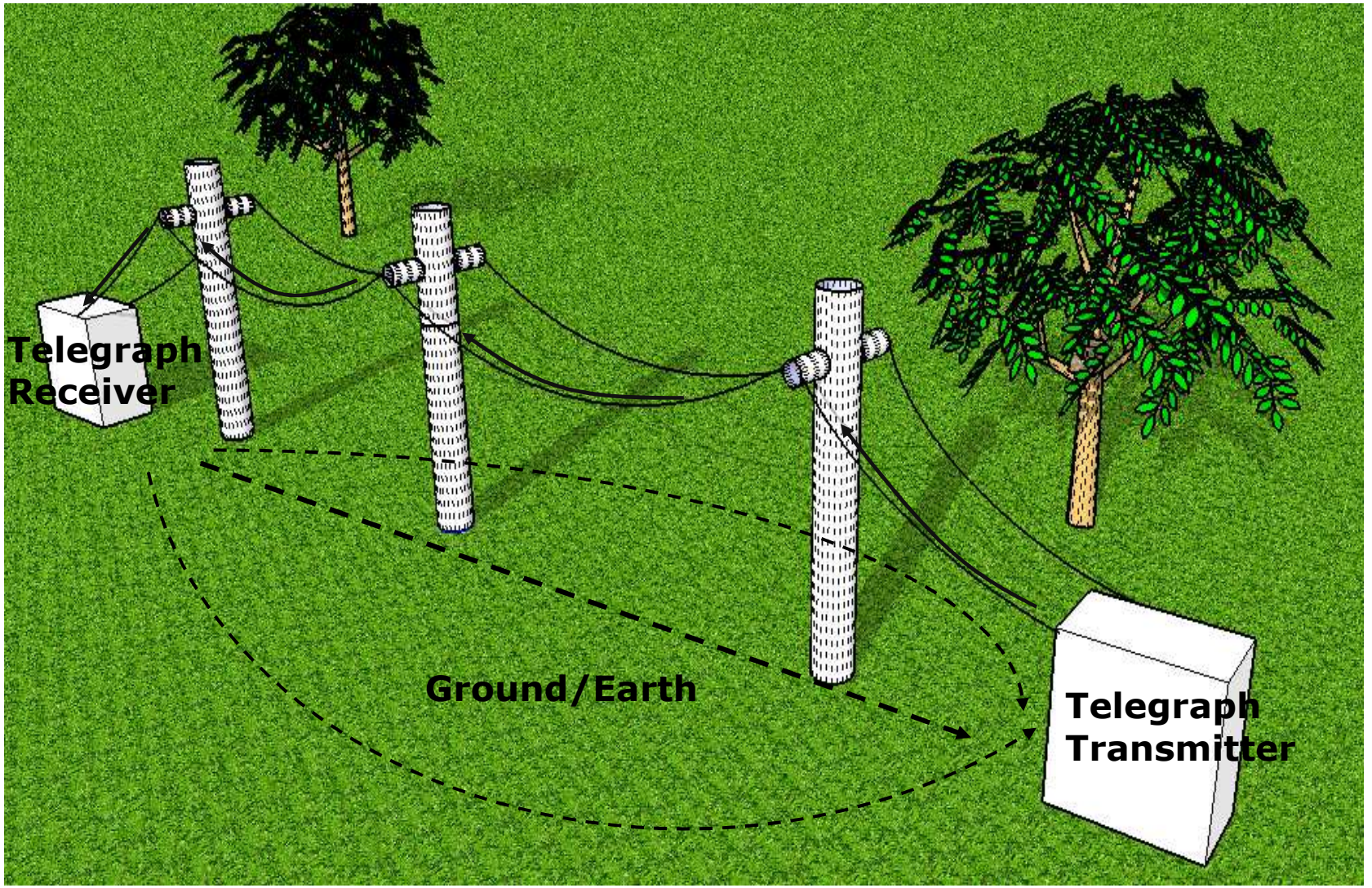
Can You Identify the EMC Problem from this Schematic?

No. We need to know the full current path, which is dependent on layout and frequency.



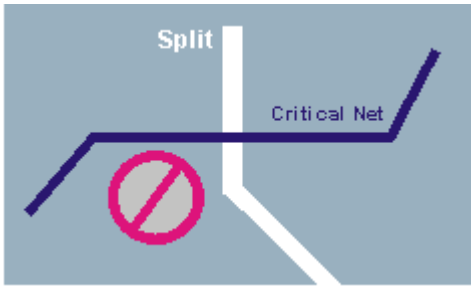

Telegraph
Receiver
Ground/Earth
Telegraph
Transmitter

EMC PCB Design Rules

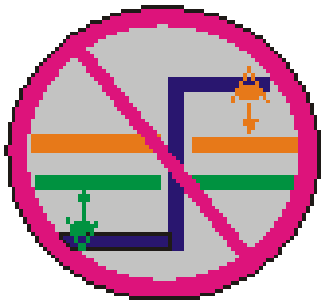
- Examples of EMC design guidelines
  - Don’t cross splits in reference planes
  - Don’t route nets too close to the edge of a reference plane
  - Bury clock nets and other high energy sources
  - Put filters on I/O lines near the connector
  - Place decoupling near IC power pins
  - Use spatial decoupling to avoid lower-frequency power plane resonances
- List grows with lessons learned
  - Importance of root-cause analysis and feedback
- New rules are needed as technology evolves (higher frequencies, move toward differential signaling, etc)
- Some rules lose importance over time

Signal Reference Rules

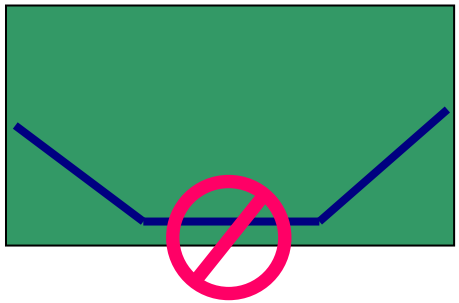
- Critical nets must not cross a split in the adjacent reference plane



- Critical nets must not change reference planes



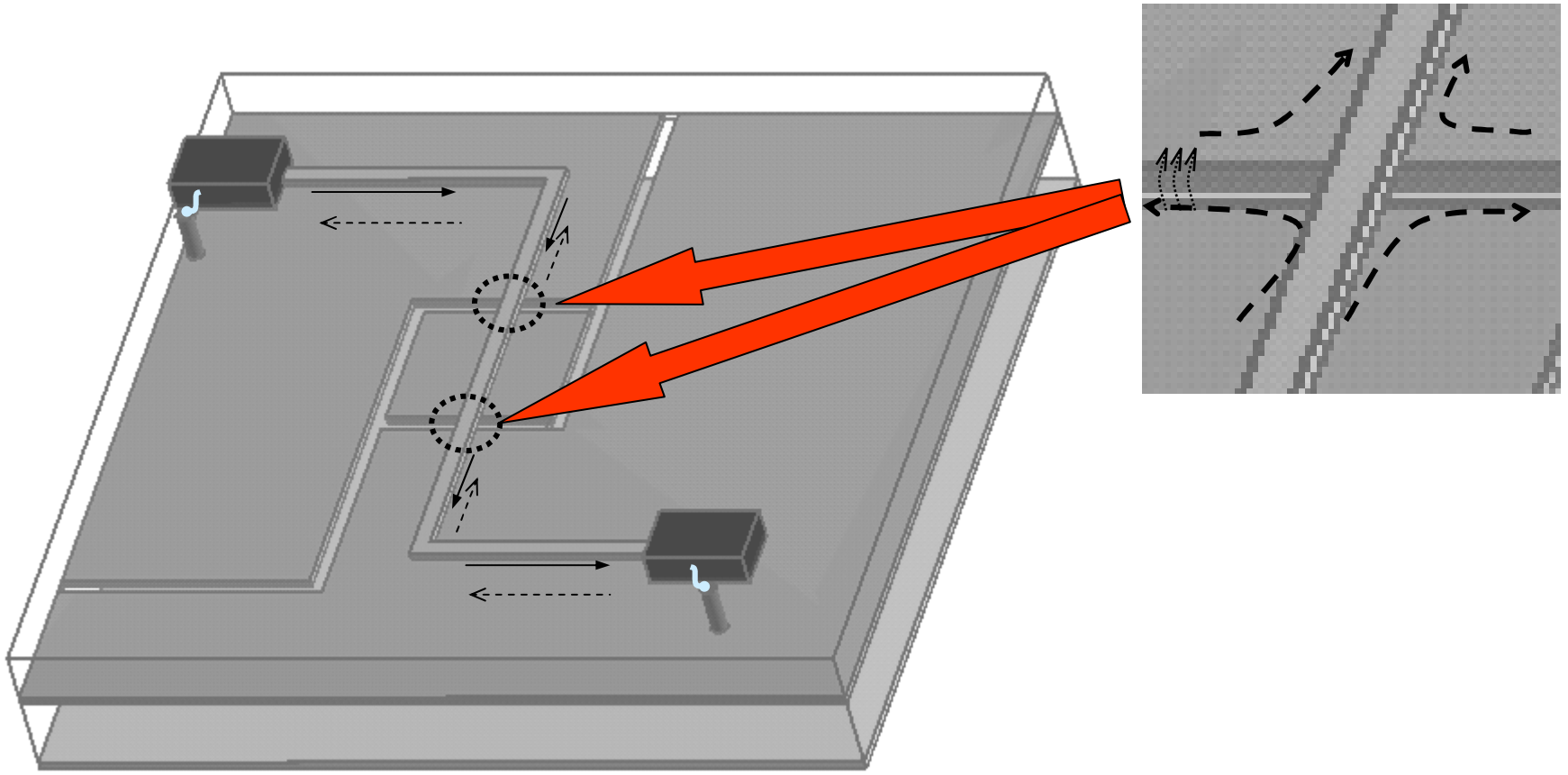
- Critical nets must not be within a specified distance of the edge of their reference plane



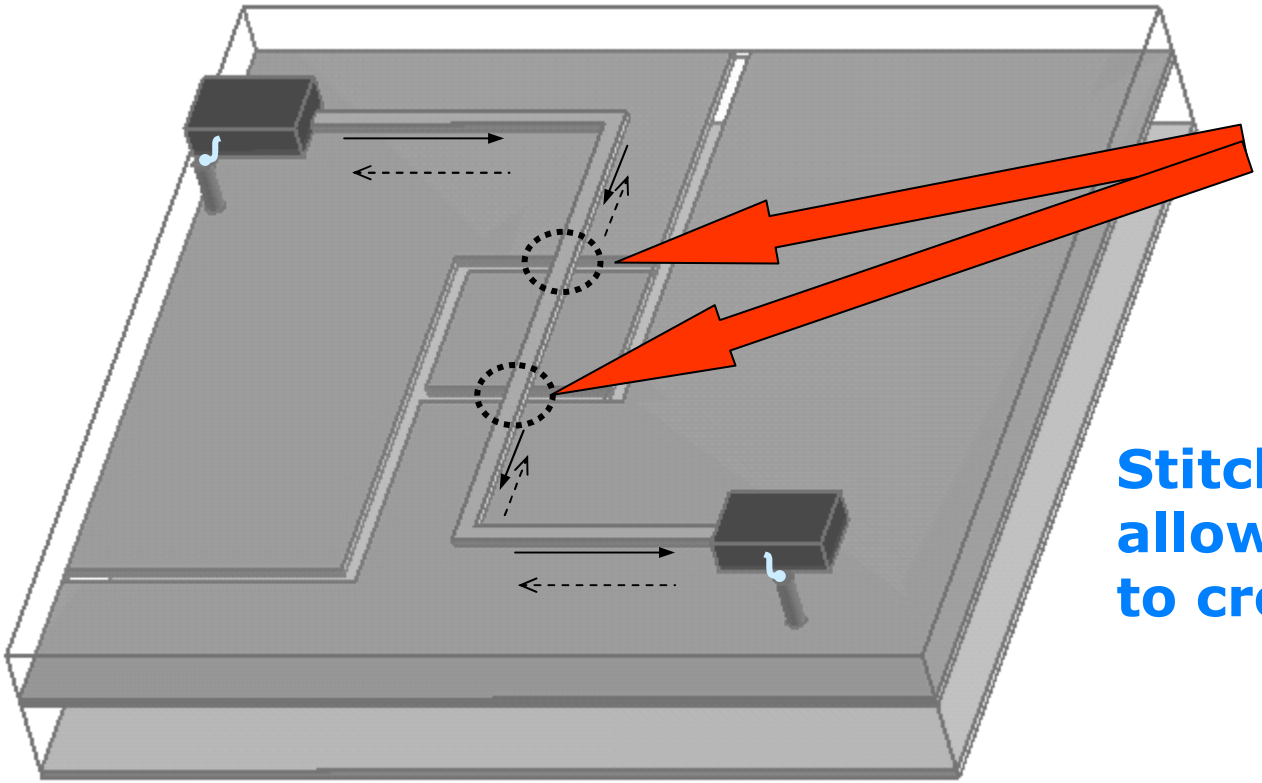
Splits in Reference Plane

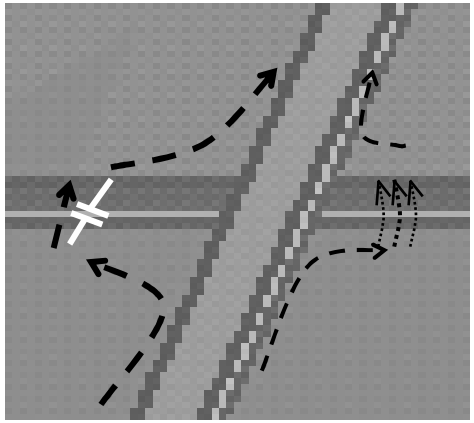
- Boards with multiple power planes often have splits
  - Sometime crossing cannot be avoided
  - Return current path is interrupted
- Stitching capacitor required across split to allow return current flow
  - Must be close to crossing point
  - Consider stitching capacitor impedance
    - Inductance dominates
- Frequency spectrum of signal is important
  - Clock signals (energy at high harmonics)
  - High frequency harmonics return through displacement current in dielectric

Split Reference Plane Example



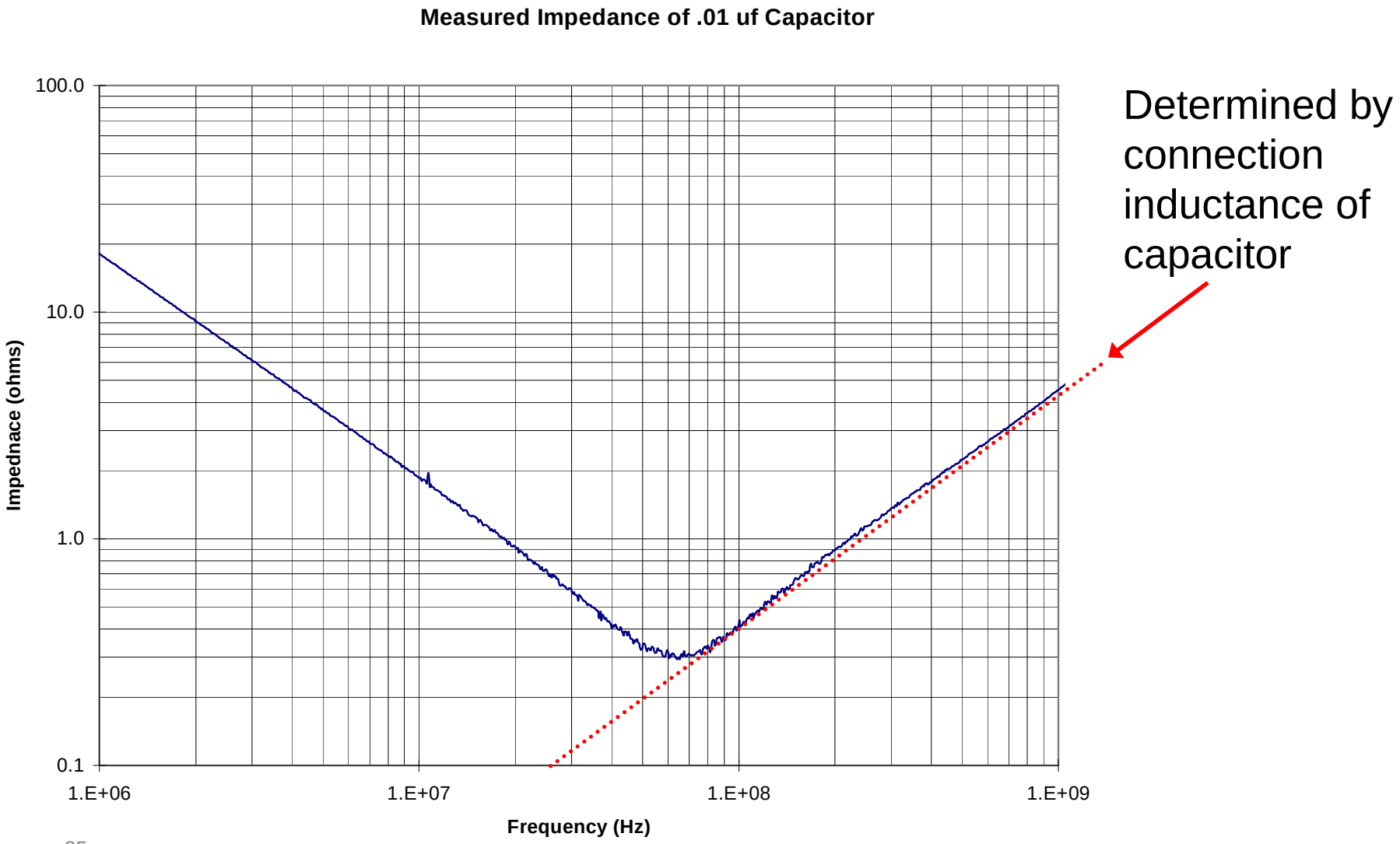
Split Reference Plane Example
With Stitching Capacitors



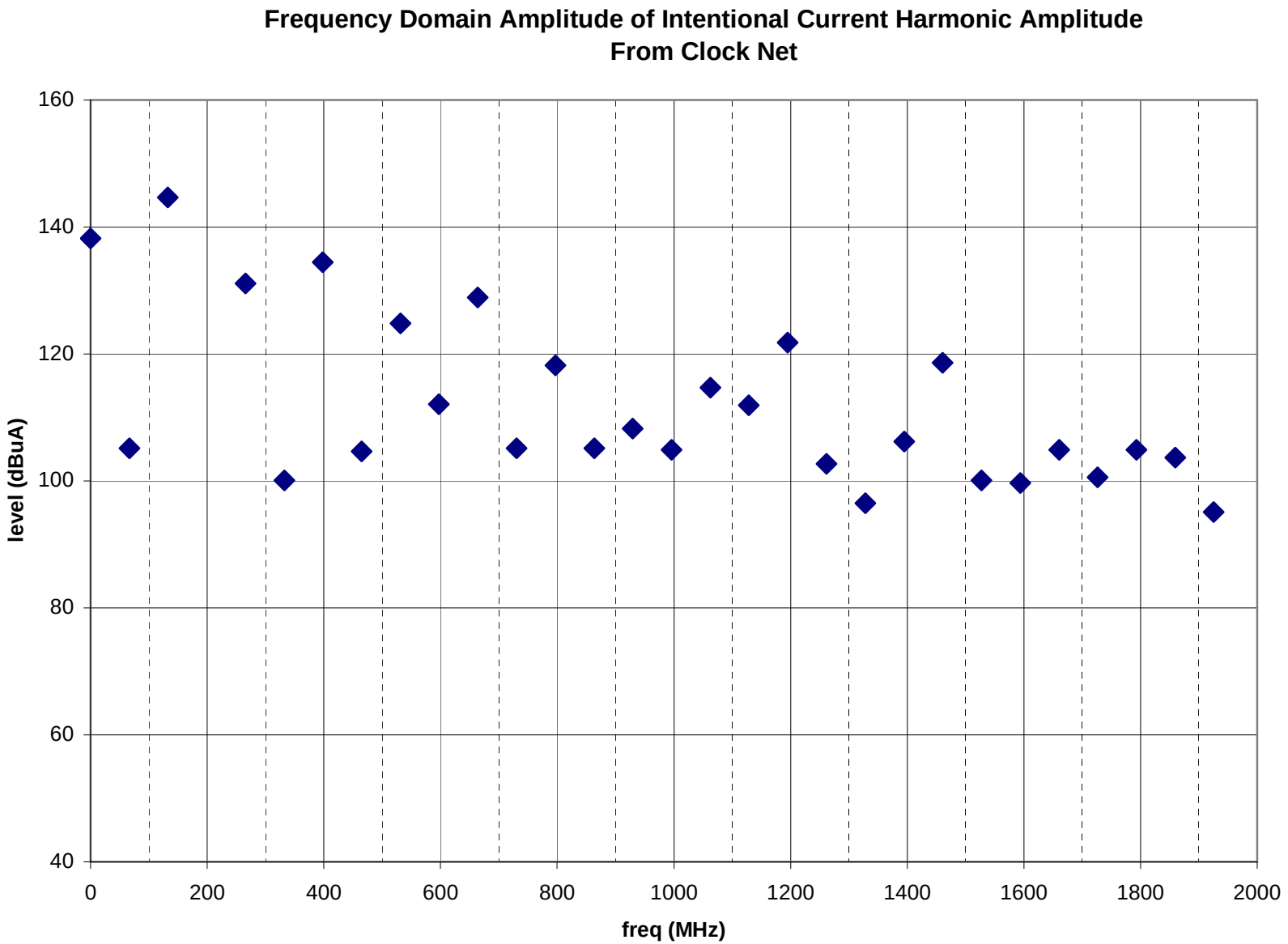


Stitching Capacitors allow return current to cross splits

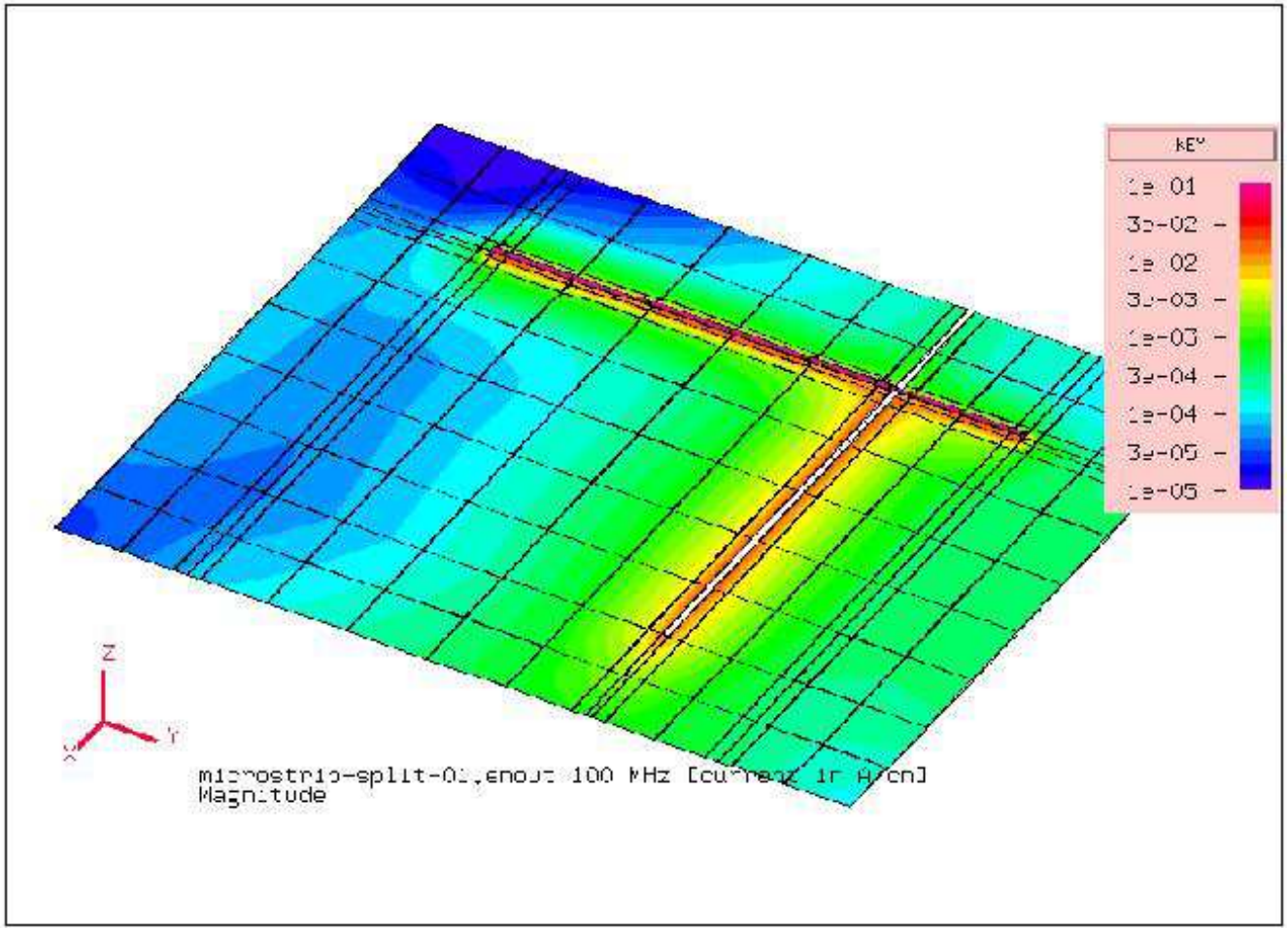
Capacitor Impedance



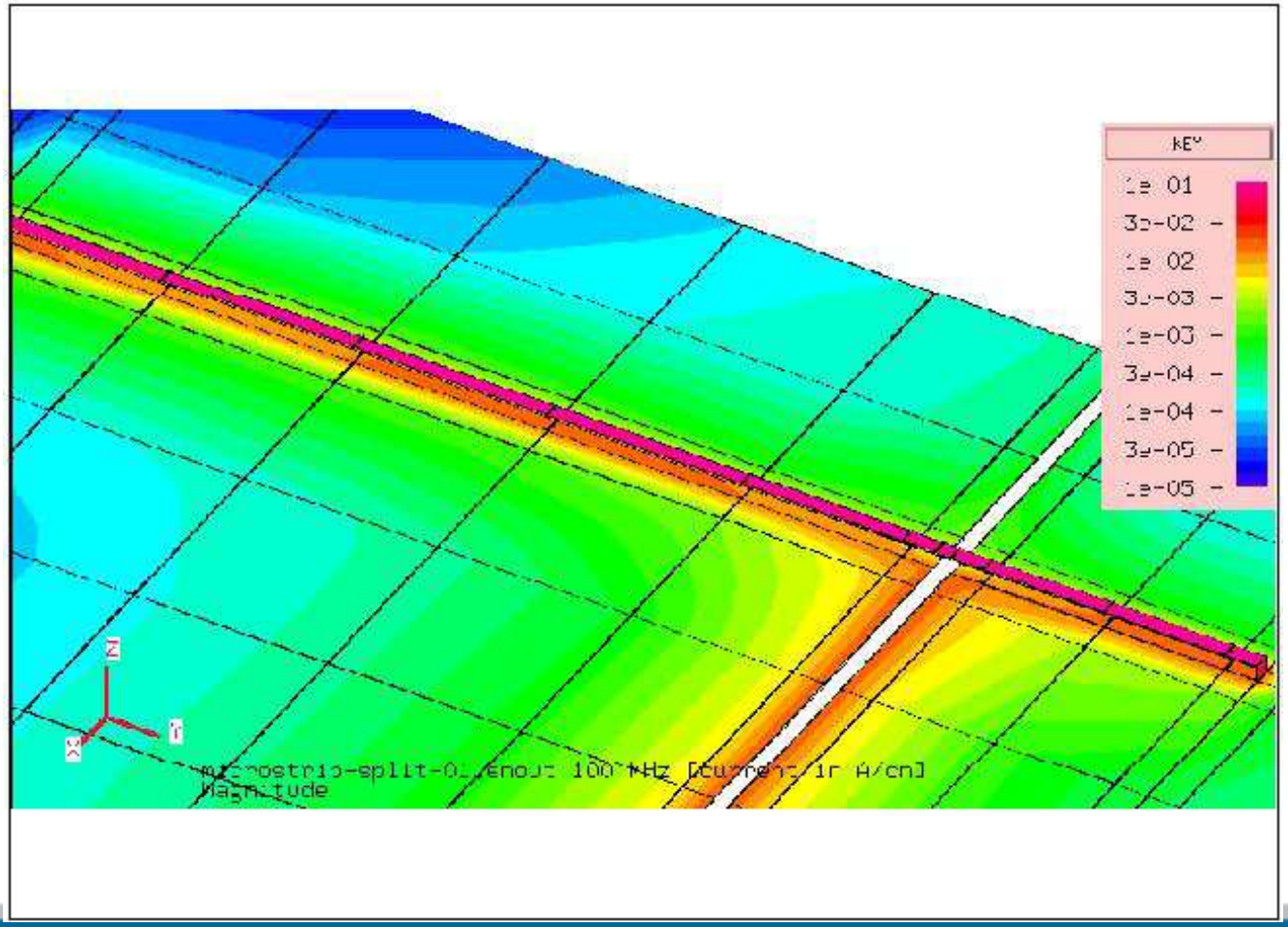
Determined by connection inductance of capacitor


Frequency Domain Amplitude of Intentional Current Harmonic Amplitude From Clock Net
level (dBuA)
160
140
120
100
80
60
40
0
200
400
600
800
1000
1200
1400
1600
1800
2000
freq (MHz)

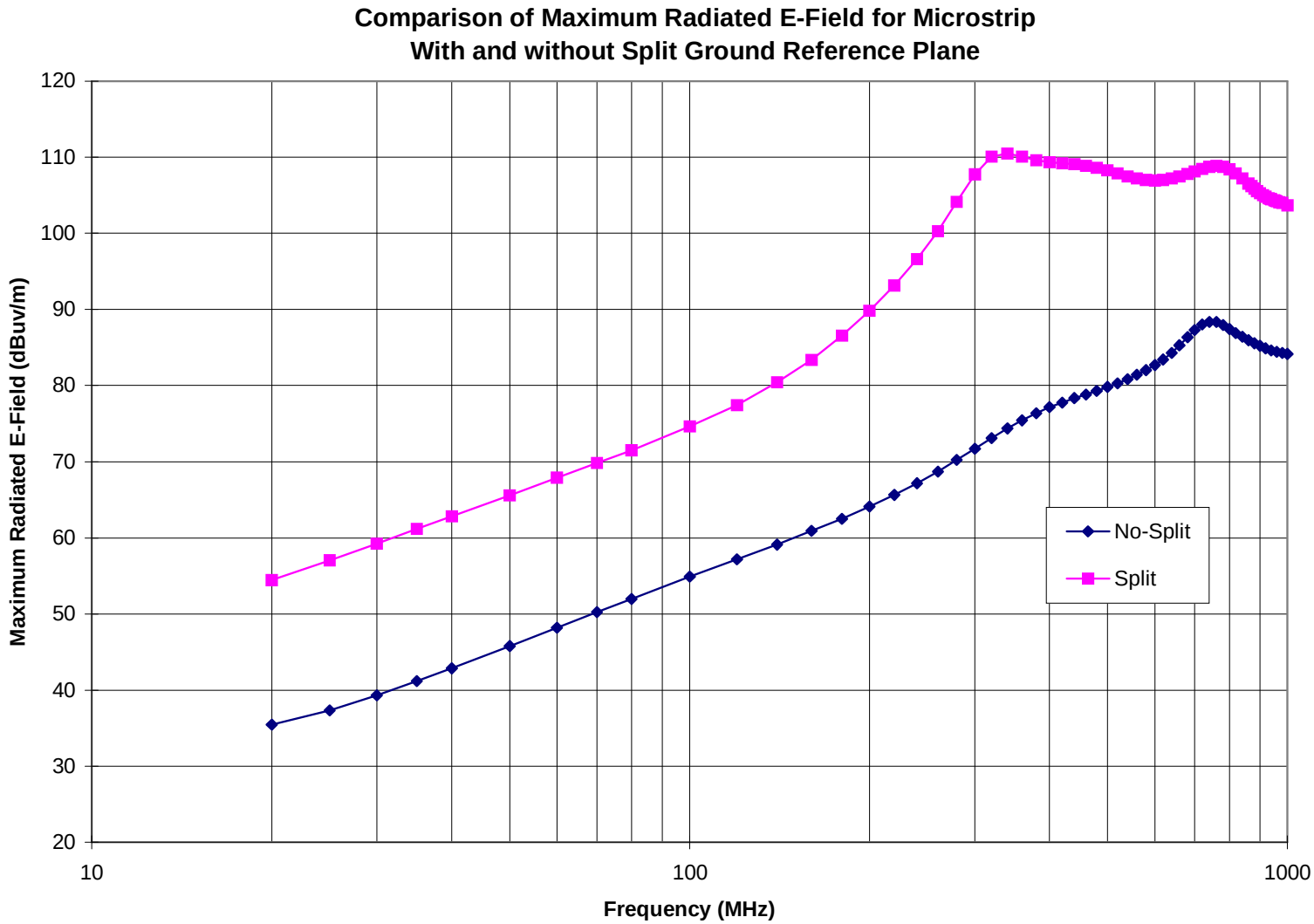
Microstrip Current Distribution Example – Method of Moments Simulation (100 MHz Clock)



Microstrip Current Distribution Example – Zoomed View

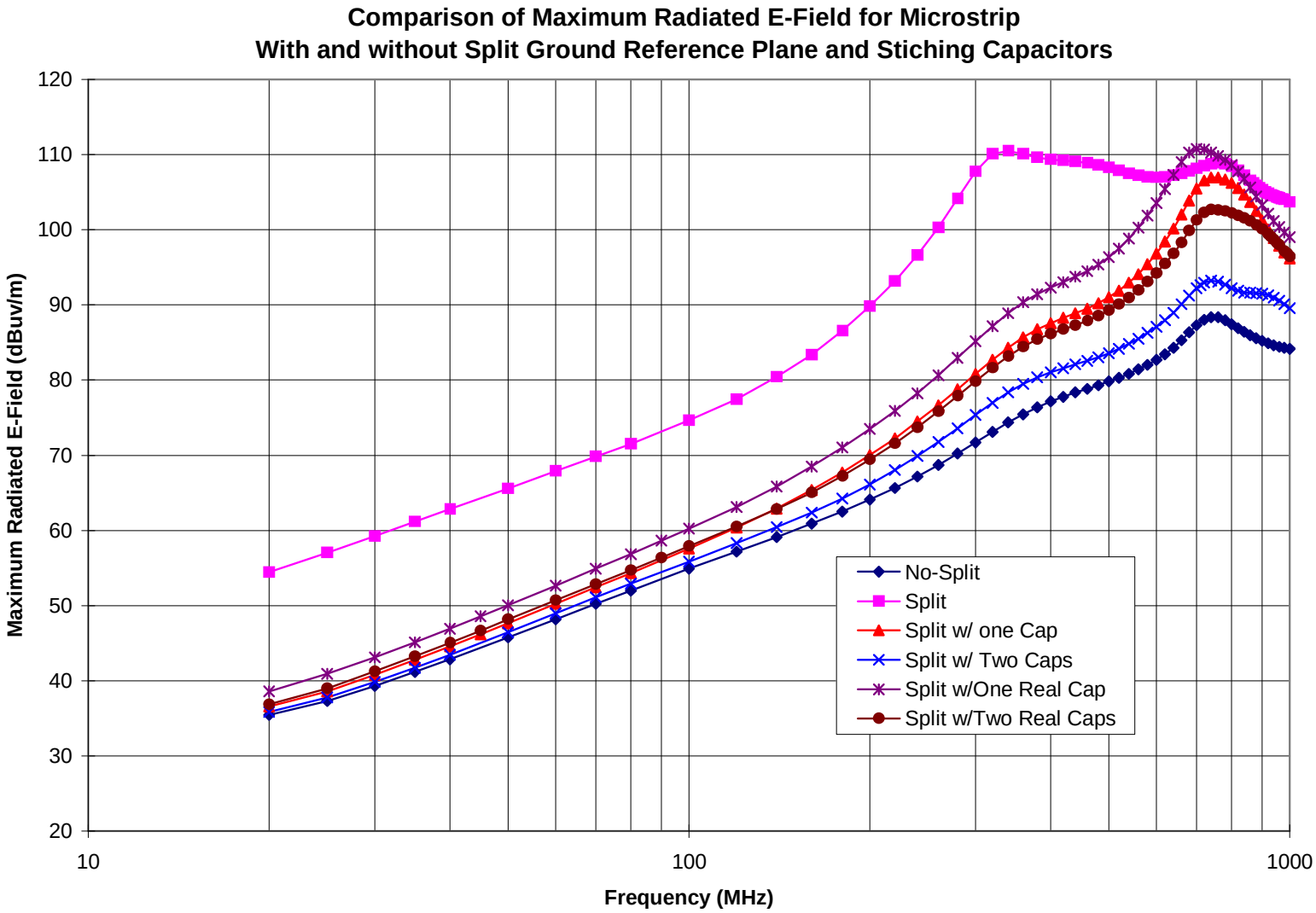


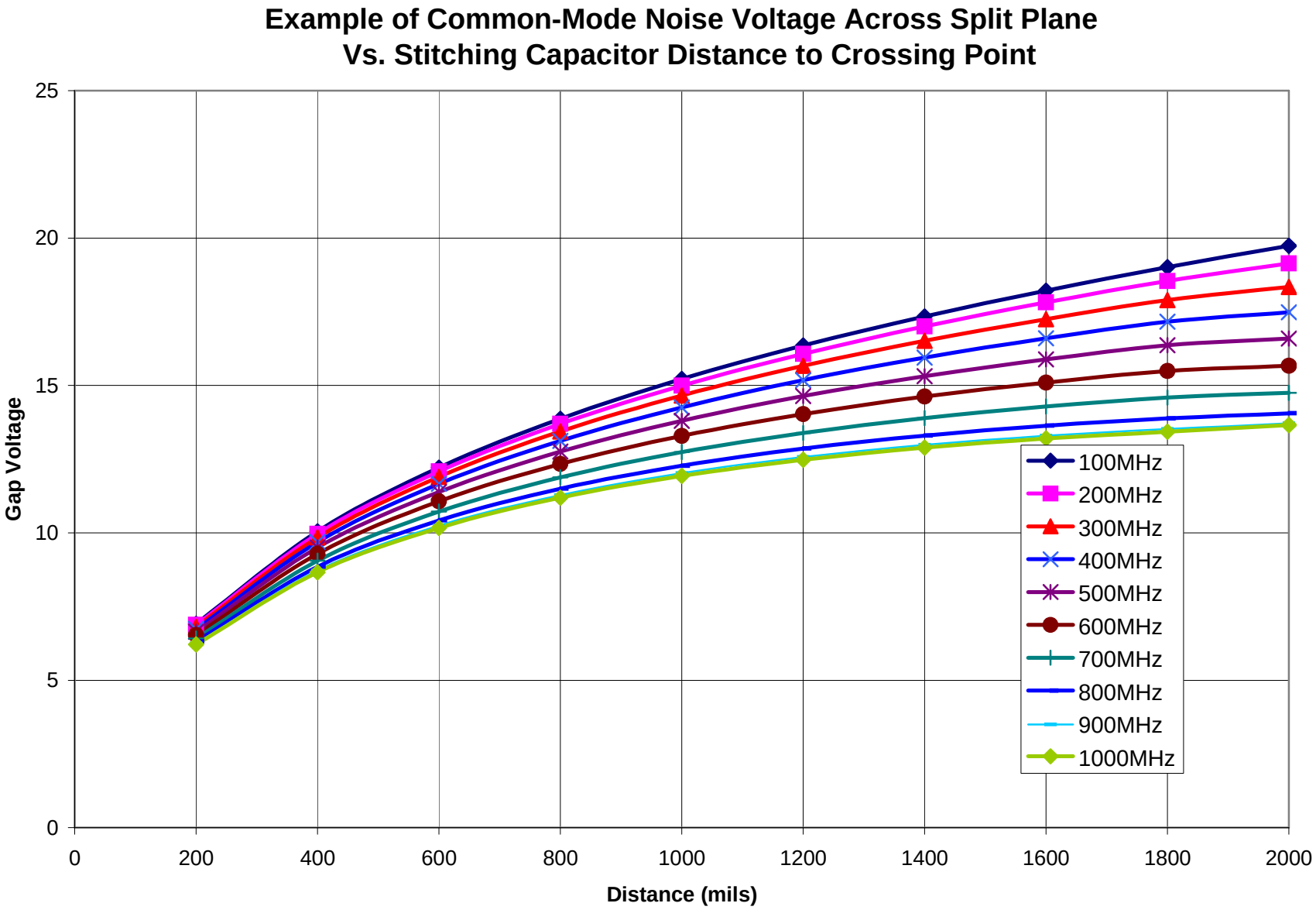
Near Field Radiation from Microstrip on Board with Split in Reference Plane



With "Perfectly Connected" Stitching Capacitors Across Split

Stitching Caps with Via Inductance



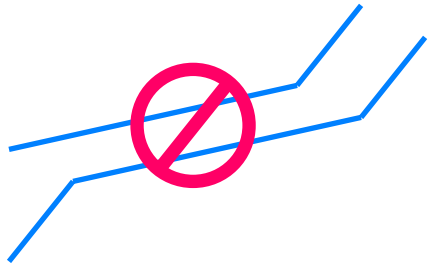

Example of Common-Mode Noise Voltage Across Split Plane
Vs. Stitching Capacitor Distance to Crossing Point
Gap Voltage
25
20
15
10
5
0
0
200
400
600
800
1000
1200
1400
1600
1800
2000
Distance (mils)
100MHz
200MHz
300MHz
400MHz
500MHz
600MHz
700MHz
800MHz
900MHz
1000MHz

Are Stitching Capacitors Effective?

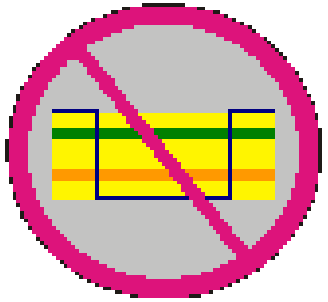
- It depends
  - Yes, at low frequencies
  - No, at high frequencies
- Limit the high frequency current spectrum
  - Slew rate control
- Avoid split crossings with ALL high-speed (high data rate and/or fast rise time) signals

Wiring and Crosstalk Rules

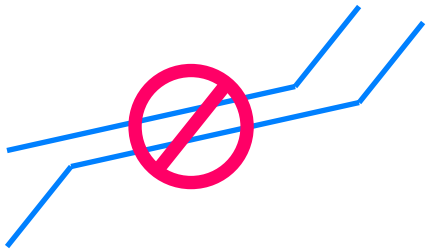
- Critical nets must not be routed within a specified distance from an I/O net



- Critical nets must be buried between solid planes

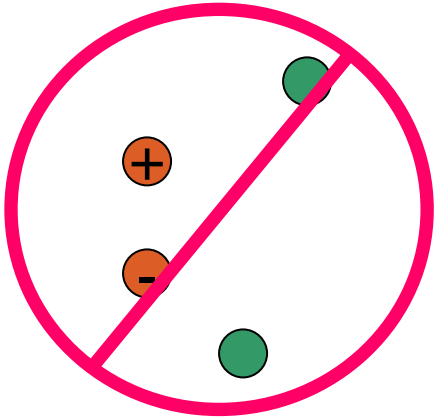


- Critical nets must be isolated from other nets by a specified distance

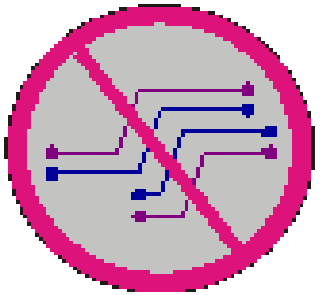


Differential Wiring and Mode Conversion Rules

- Differential vias must have symmetrically placed return vias

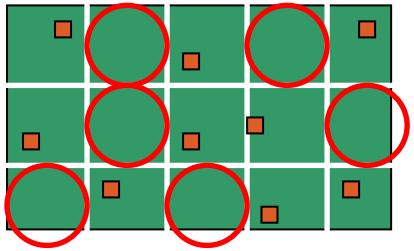


- Differential critical nets must be routed within a specified distance of each other, and the length of the mates must match within a specified amount (running skew)

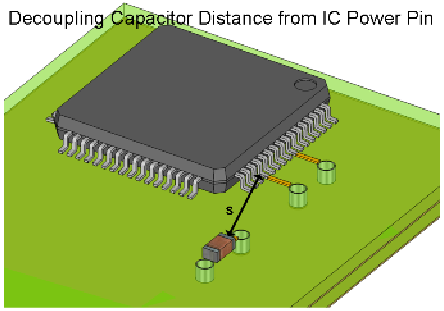


Decoupling Rules

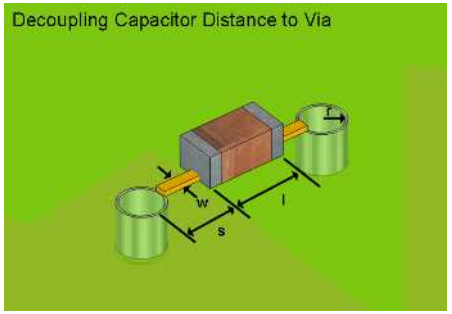
- Decoupling capacitors must be placed between all adjacent plane pairs within a specified grid density (spatial decoupling)



- A decoupling capacitor must be placed within a specified distance from each IC power pin

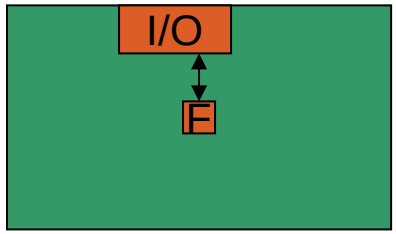


- The trace connecting between a capacitor (or IC) pin and its via to the power/ground-reference plane must be no longer than the specified distance

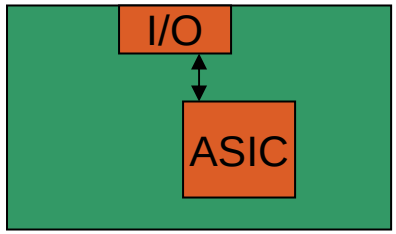


Placement Rules

- Filters must be placed close to the I/O connector pins they are filtering



- Certain devices must be placed a specified distance away from other devices or from I/O connectors
  - Analog and digital isolation
  - Prevent coupling of ASIC emissions to I/O signals

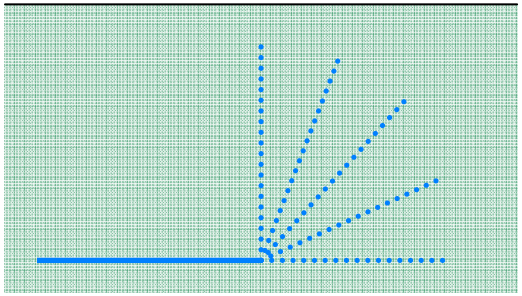


Evolution of Design Practices

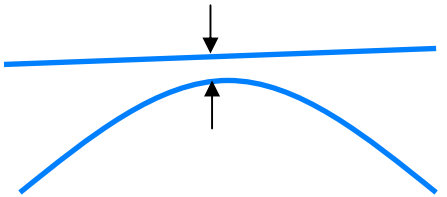
- Technology evolves
  - Higher frequencies (data rates and rise times)
  - Higher density (smaller components, better process control)
  - CAD program enhancements
- Design rules must adapt
  - Update models & analytical formulae
  - Build new test vehicles

Design Evolution Example 1

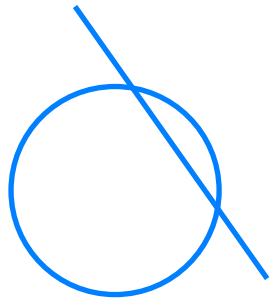
- 10 years ago, all nets were routed with straight lines
  - Also mostly at fixed angles (multiples of 22.5 degrees)
- Now, arcs are supported
  - Requires more advanced algorithms for bounding box and intersection calculations



Angle of approach to edge of plane



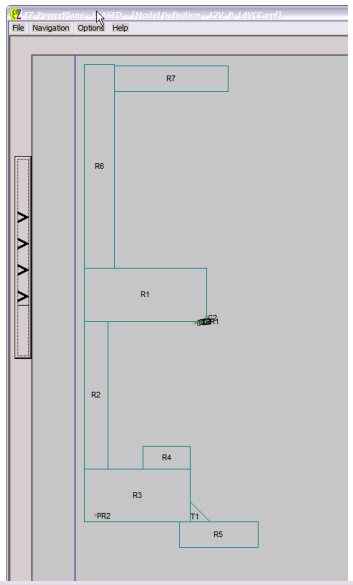
Isolation between traces



Trace over round hole

Design Evolution Example 2

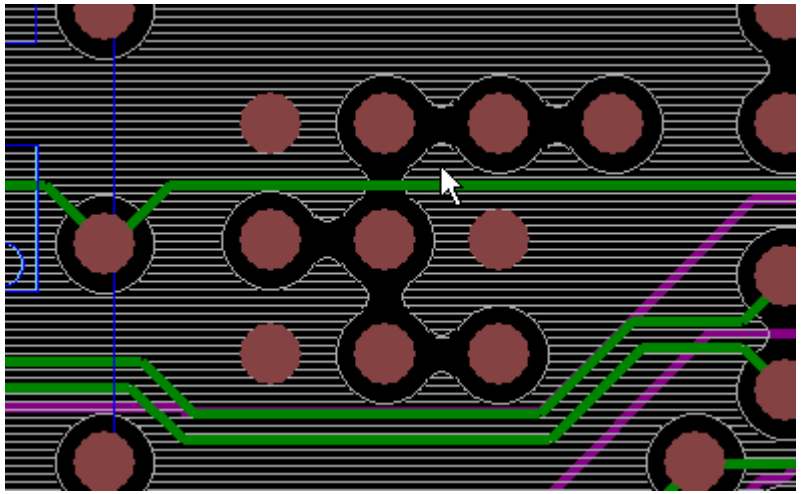
- De-emphasis or change in focus of decoupling rules
  - 10-15 years ago, spacing between power and ground planes was typically 10 mils or more
    - Smaller layer count
    - Fewer devices and lower pin count connected to planes
    - More energy content between 30-300MHz
  - Now, power planes have separations of 3-4 mils (or smaller with special dielectrics)
    - More capacitance between planes reduces dependence on decoupling caps
    - Higher frequency content does not excite the lower-order resonant modes where caps are effective
    - Higher device and pin count lowers the Q of plane resonances



Dielectric thickness dropped from 10 to 4 mils = ~8 dB drop in impedance

Design Evolution Example 3

- Shrinking features, such as pin pitch, create new challenges
  - When antipads overlap, they create a slot in reference plane
  - If CAD data does not join antipads, then rule-checking tool must do it



Design Evolution – Other Examples

- Vias
  - Back-drilling
  - Blind
  - Shared antipad
- Nets
  - Linked nets (i.e. through DC blocking caps or series resistors)
- Layers
  - Embedded capacitance (non-uniform dielectric through stackup)
  - Power/ground shapes on signal layers

Summary

- PCB design for EMC is all about currents
  - Pay attention to return current path
- Design rules are needed to achieve EMC compliance
- Main EMC design rules are well known
  - Numerous publications & presentations
  - Use simulation and measurement results to select meaningful limits
- As technology changes, rules need to adapt

Present State of Automated EMC Design Rule Checking

Rule Checking Choices

- Automated vs Manual Reviews
- Develop vs Purchase
- Level of analysis

Progression of EMC PCB Design Rule Checking

- From light tables and transparencies to CAD reviews
  - Rule checking findings migrate from hardcopy to softcopy
- From co-located teams to global teams
  - Harder to conduct manual reviews and communicate issues to designer
- From low layer count and low density boards to high layer count and high density boards
  - Too complex to review manually within time constraints
- From manual reviews to automated reviews

Automated Reviews

- Pros
  - Saves analysis time
  - More repeatable
  - Less prone to human error
  - Psychological factor (facts vs opinions)

- Cons
  - Have to learn a new tool
  - Development or purchase expense
  - “If we buy a tool, they won’t need me”

Develop vs Purchase

- Develop
  - Have resources to develop algorithms and software
  - Need something special
    - Custom-tailored to your design process
    - Conversion or pre-processing of CAD data
- Purchase
  - Need a solution today
  - Don’t have mix of CAD and software skills available
  - Flexible design process
  - NB: Some tools allow customization

Purchase Options

- The major CAD vendors have a rule checking solution
  - Pros:
    - Integrated in design tool
    - Easy to adopt
  - Things to check:
    - Can it process boards from other vendors?
    - Is the tool supported and maintained by knowledgeable EMC engineers?
    - Can the rules and limits be customized?
    - Cost
- 3rd Party Vendors
  - Pros:
    - Rule checking is main focus, not a supplementary tool
    - Supported and maintained by knowledgeable EMC engineers
    - Support multiple CAD formats
  - Things to check:
    - Can the rules and limits be customized?
    - How easily will the tool fit into your design process?
    - Cost

Level of Analysis

- Simple geometrical design rule check
  - Very fast
  - Straight-forward to use and interpret
- "Expert System" analysis
  - Moderate speed
  - More complicated calculations
  - Attempts to provide more guidance on whether to fix a problem and how
  - Requires understanding of assumptions and limitations

Rule Check vs. Expert System Example

- Avoid Exposed (Microstrip) Traces
  - Rule Check
    - Set a limit on total exposed length
  - Expert System
    - Calculate field strength at 3m/10m away based on radiation from a microstrip
      - What if 2” are exposed on each end? Does radiation add?
      - What if the PCB has a shield around it?
      - What frequency(ies) are calculated?

Rule Checking Capabilities

- Rule configuration
- Design classification
- Results
  - Reports
  - Visualization of violations

Rule Configuration

- Tool must provide an intuitive way to:
  - Define your “playlist”
    - Which rules to run
  - Define your rule limits
  - Define which options are enabled
    - Adjustments to how the rule works
  - Store and recall settings

Design Classification

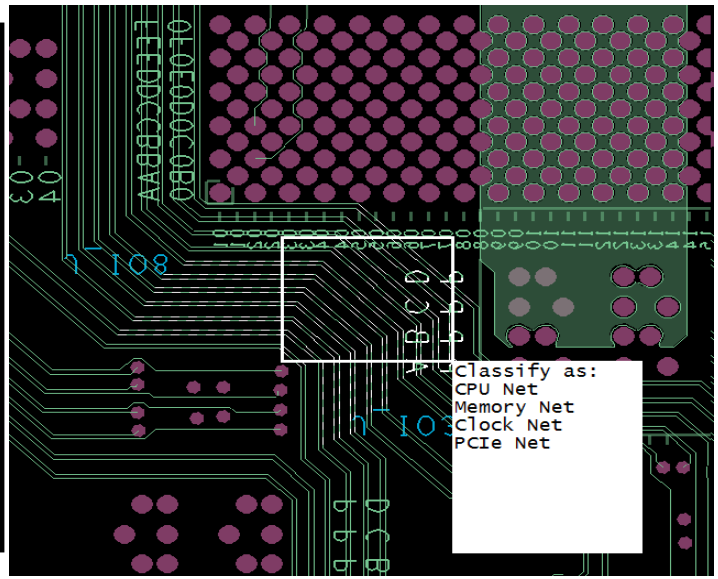
Control File:

CPU* = CPU Nets

CLK = Clock Nets

DDR* = Mem Nets

P*_DD* = PCIe Nets

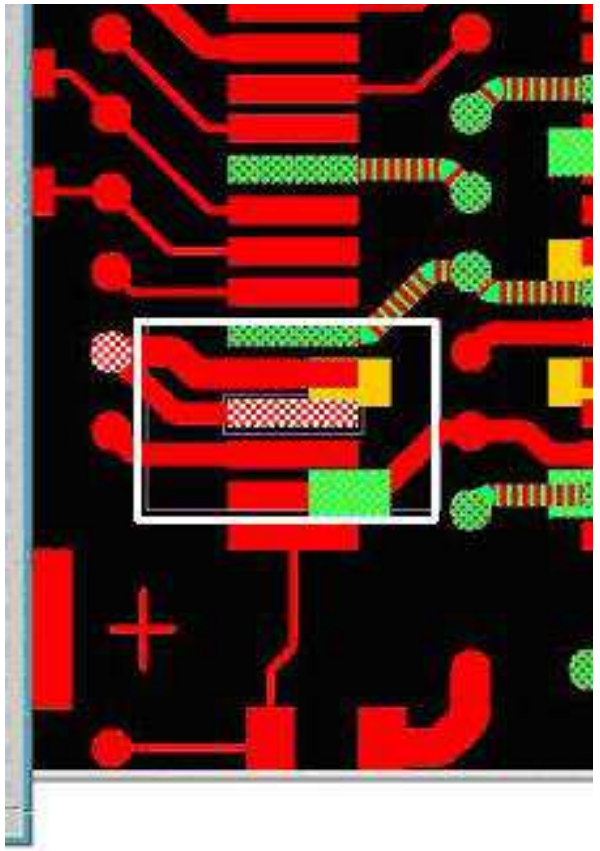


Net Name	Clock Nets	CPU Nets	Mem Nets	PCIe Nets
CPU_ D01		X		
CPU_ CLK_P	X	X		
DDR_ DQ01			X	
P01_ DD01				X

- Tool must provide an intuitive way to define which nets and components are important
  - Automatically classify by naming convention
  - Manually classify by selection within graphical interface (CAD tool)
  - Manually classify in a spreadsheet-like interface

Results

- Tool must provide a way to review violations
  - Convenient report format that can be sent to team members
    - Standard formats are usually best (HTML, PDF, XLS, ODF, etc)
  - Visual display provides best context for decision making



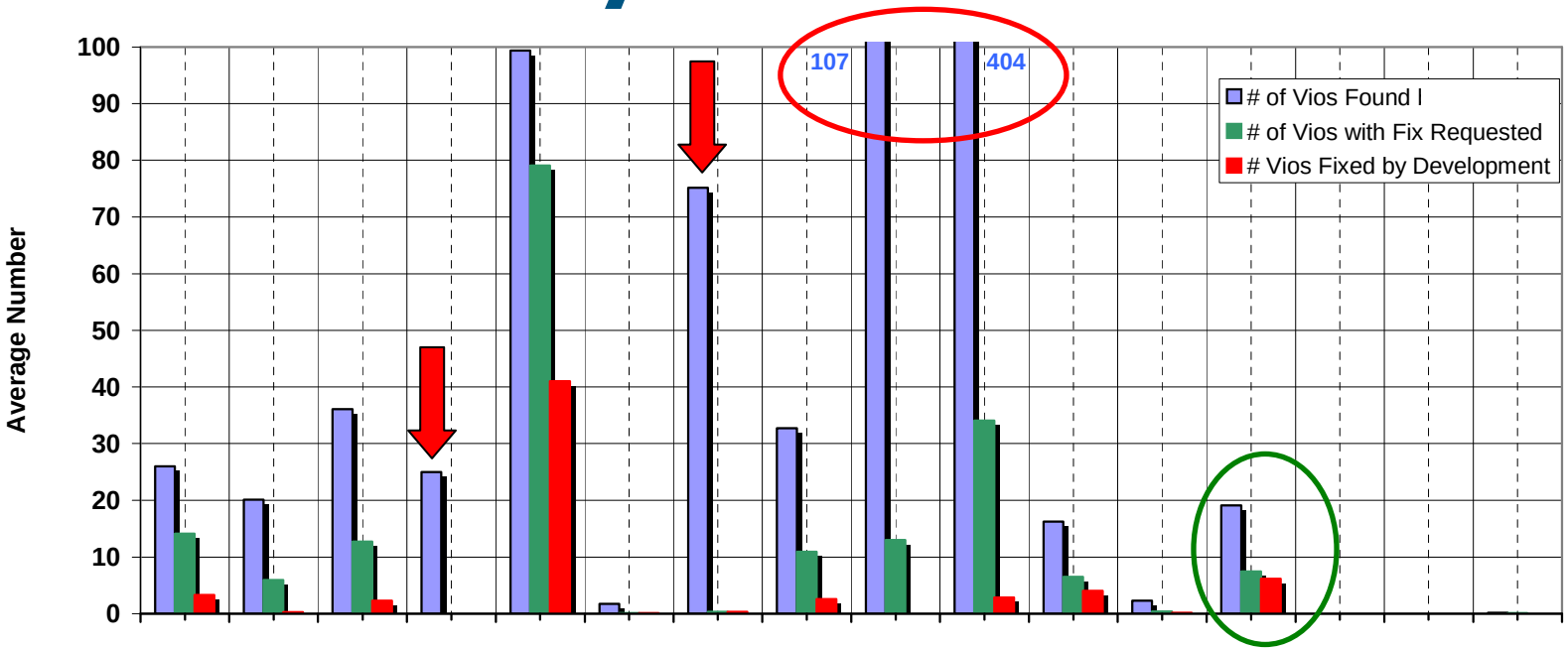
Rule Checking Application Considerations

- Modularity and Expandability
  - **Ability to add and modify rules easily to adjust to technology changes**
  - Support for multiple CAD formats
- Measurability
  - Might need/want to track usage
  - Data mining of results statistics can be used to improve rules
- Usability
  - Does it have to run inside the CAD environment or can it be a separate process?
  - How does the user review output?
- Portability
  - Support for multiple operating systems
- Maintainability
  - Use a modern language (balance of what skills are present in your organization and availability of compilers, libraries, etc)
  - Object-oriented design

Modularity and Expandability

- Easy to add new rules
  - Adapt to technology changes
  - Incorporate other rulesets
    - Signal Integrity
    - Power Integrity
    - Thermal? Mechanical? Other?
- Easy to adjust settings and limits for rules
  - No recompiling or modifying of scripts required

Measurability



- Continual process improvement is key
- Benefits:
  - Measurable improvements to tool
  - More effective usage of tool
- Note:
  - Minimize extra work for users (make it easy!)

Summary

- Automate!
  - Speed
  - Consistency
- When selecting a tool or developing one
  - Be wary of "expert" tools that apply algorithms beyond their scope
  - Choose flexibility
    - Ease of adding and customizing rules
  - Consider integration with design process
    - Setup, rule execution, and results evaluation
    - Tracking

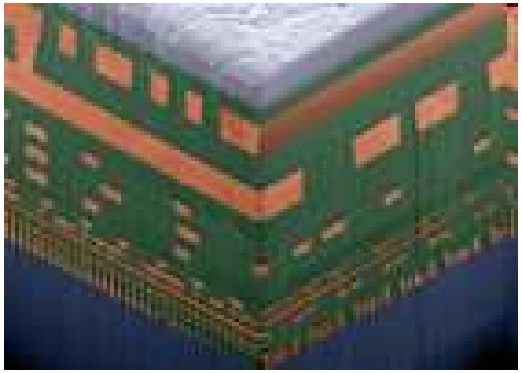
Future of Automated EMC Design Rule Checking

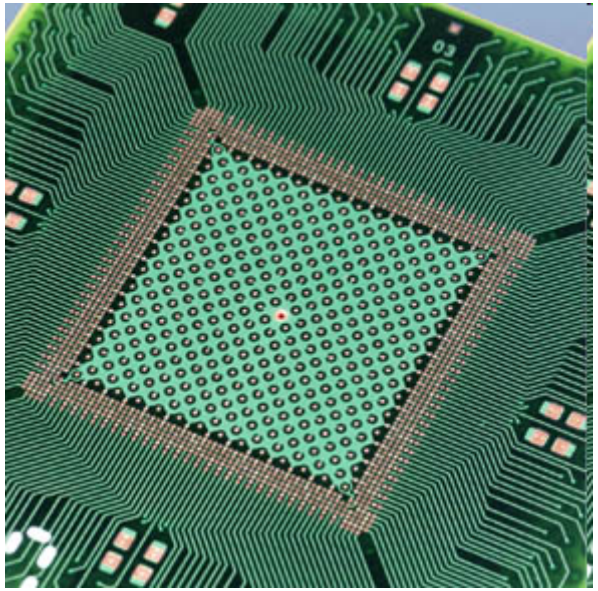
Computing Paradigm Shift

- Cloud computing
  - Advantages:
    - Tools pre-loaded and pre-configured in a virtual instance
    - Shared rule and design resources
    - Offload computationally intensive analyses
    - Enables usage tracking
  - Issues:
    - Graphics performance over web interface
    - Licensing for CAD tools
    - Intellectual property security concerns

Design Rule Checking for ASIC Packages

- Organic packages are small PCBs
- Packages are electrically large above 3 GHz (10cm wavelength)
- With each new silicon technology family:
  - Smaller gate sizes
  - Faster slew rates
  - Higher emissions





Previous Work on EMC of ICs

- Measure near-fields above IC
  - Find design patterns that cause “hot-spots”
  - Convert to equivalent dipole sources and predict far-field radiation
  - Issues:
    - Can you measure near-fields with lid on?
    - What if the IC needs a heatsink to operate with normal traffic?
    - Helps with system-level simulations and design, but usually too late to impact IC design

Common Threads in Recent Literature

- PCB-Package Co-Simulation
  - Include package parasitics in end-to-end link simulations
  - Marry PDN characteristics of both domains to get total picture of power delivery to chip
- SI-PI Co-simulation
  - Include power integrity effects in signal integrity simulations

- Where is EMI is this discussion?
  - EMI tends to be ~20dB more sensitive than SI

Rules to Explore

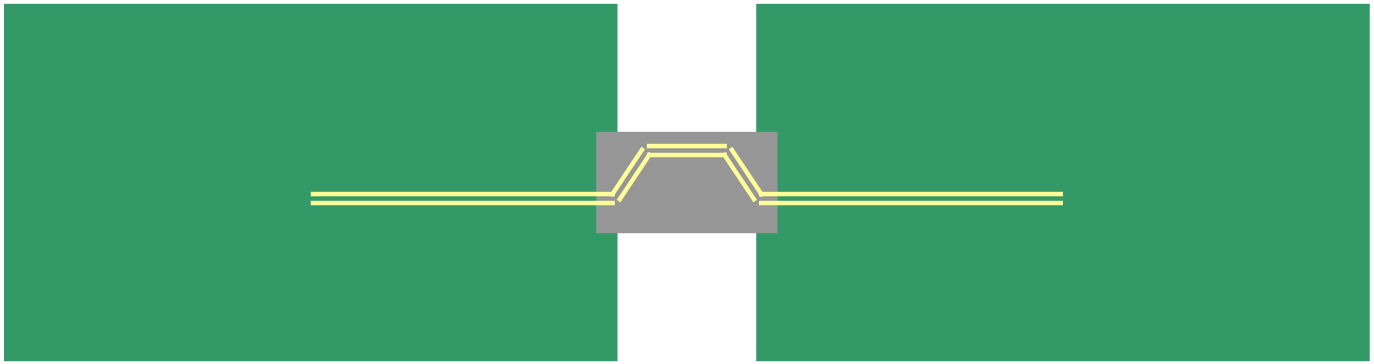
- Decoupling rules for package
  - Via stitching and decoupling between planes
  - Adequate number of BGAs between PCB and package for power and ground nets
- PCB wiring rules applied to package
  - Signal referencing
    - Splits
    - Reference plane changes
  - Signals buried and away from edges of planes
  - Differential Pair Skew
- Lid grounding
- Other?

Design Rule Checking for Systems

- Most existing rule checking tools and efforts focus on PCBs
- Many issues found in the lab are caused by mechanical or system integration issues
  - Missing or ill-fitting gaskets
  - Cables and connectors between PCBs
  - Grounding

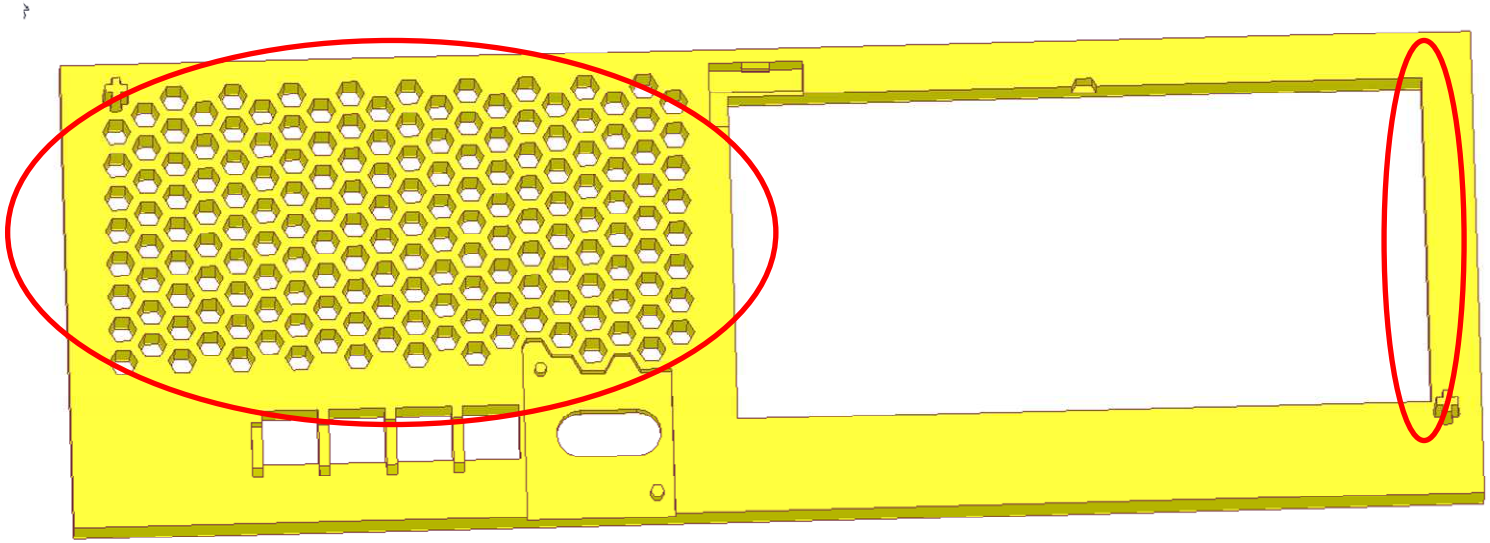
Design Rule Checking for Systems

- Extend PCB rules to multi-board scenarios (running skew, signal reference continuity, I/O filter placement)



Design Rule Checking for Systems

- Work on ways to process mechanical CAD files and identify holes, slots with missing gaskets, other

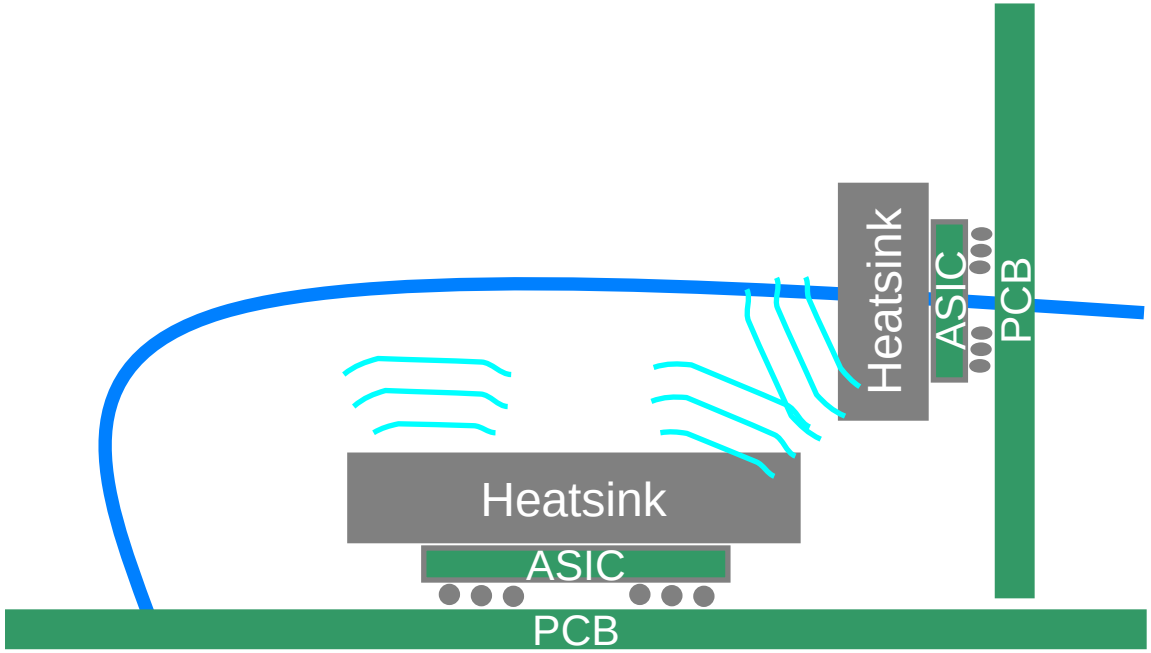


Challenges of Mechanical Rule Checks

- Supporting multiple CAD formats
- Modularity
- Tolerances
- Metal coatings
- 3D vs “2.5D”

Design Rule Checking for Systems

- Combine electrical and mechanical design data and evaluate grounding, excessive coupling between parts



Design Rule Checking for Systems

- Develop way to visualize problems for easy reviewing
  - Standard formats
    - STEP
    - 3D-PDF
    - U3D
  - Embedded in CAD tool with scripts

Summary

- Time to move beyond checking individual PCBs
- Cloud computing opens new possibilities
- Rule-checking at IC package level
  - IC packages are small PCBs
  - ICs are not electrically small above 3-5 GHz
  - Many PCB design rules apply directly
- Rule-checking at System level
  - Many EMC issues are related to system integration
    - Check mechanical features
    - Check electrical-to-electrical, electrical-to-mechanical, and mechanical-to-mechanical interfaces