EMC Design Risk Assessment

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Introduction

Products are occasionally subject to minor modifications after EMC compliance testing has been performed. A complete retest may seem excessively expensive in relation to the required modification (maybe a resistor change or moving of a track on a PCB), hence the product supplier may decide not to retest (if self-certified this is permissible). In cases of very minor changes this will be an acceptable approach as the change is unlikely to effect the EMC performance, but if a product did prove to fail its EMC requirements at a later date, could the company show due diligence in omitting to retest without recorded evidence that they had considered the effect of any design changes?

Presented here is an EMC design risk assessment (EDRA) technique that provides both a qualitative and quantitative technique for assessing the impact of individual product design changes on the compliance status of a product. The technique is based on Design Failure Mode and Effect Analysis (DFMEA), a method used extensively in the aerospace and automotive electronics industries and consequently should be familiar to engineers who have worked in these areas. A basis in existing engineering practice should enable the technique to gain some credibility with DFMEA proponents as well as offering newcomers to the technique some confidence that the methodology has a precedent in other areas.

EMC Test Results

The results of successful EMC compliance tests are hopefully familiar to readers of this journal; typically results consist of spectra of emissions with limit lines and simple “pass” for the immunity and ESD tests with their applied test levels and applicable standards. The emission results can make assessing the effect of a design change relatively easy (particularly if there is a lot of headroom between the measured result and the limit line). Lack of quantitative detail from immunity and ESD testing makes it difficult to assess the impact of design changes on these parameters.

Risk and Impact

The use of existing knowledge of the effect of minor design changes, from the experiences of multiple projects and the collective experience of many different designs (and designers), allows a simple qualitative assessment of the risk of these changes and their relative effect on the EMC performance of any given design. There is an additional impact assessment that can be used to determine the likely measurable effect of the change, based on the application/location within EMC critical circuits (e.g. frequency dependent or input-output circuits). The risk factors can be modified to apply to specific industries (telecommunications, automotive, white goods etc.), but the impact assessment should be generic to all electronic modules and products.

EMC Design Risk Assessment Technique

The EDRA technique is based on 4 categories of risk (implied effect), each of the categories has numeric range to indicate level of EMC risk (table 1). The impact assessment is a simpler 3-category multiplier based on the circuit application of the change. The risk factor is multiplied by the impact factor for each proposed change.

Consequently a simple change such as a change in a bias resistor value has in itself a low risk on system EMC performance. However, if this bias resistor is connected to an I/O circuit there is the potential that this will reduce the immunity of that circuit hence has a greater impact than if this is simply holding up an unused internal logic gate. It is also important to include changes that have no implied EMC risk, such as change in temperature performance, as this demonstrates that the change was considered and assessed to have no effect.

The category values are open to discussion and may be set for specific industries, values quoted here should be appropriate for an electronic module of moderate complexity (e.g. PC plug-in card or similar sized electronic controller). Highly complex, higher component density systems (e.g. complete PC’s or instrumentation systems) may use slightly higher threshold values as higher component count systems may be less affected by single component changes.

Risk Categories;

Risk categories are based solely on the change proposed.

None: risk has no conceivable influence on the EMC or the proposed change has been tested in the circuit and proven to have no effect. An example is the use of a commercial temperature graded part rather than a military temperature part; EMC risk=0.

Low: minimal risk to EMC, other data is available to support the influence and suggests negligible impact. For example a pull-up or bias resistor value change from 5kW to 10kW; EMC risk=1, increasing a power track length by a small amount (less than 10mm); EMC risk=2, moving an interface IC closer to a connector (could actually improve emissions but worsen ESD); EMC risk=3.

Medium: a worsening in some aspects of EMC performance can be expected but not enough in any individual case to cause an increase of more than 3dB in emissions or effect immunity. Examples include reducing a bias resistor by more than 50% (i.e. reducing a 47kW to 4k7W); EMC risk=4, changing a single de-coupling capacitor by approximately 50% of its current values (i.e. using a 470nF capacitor where a 1uF had been placed or vice versa); EMC risk=5, reducing the ground plane coverage by up to 25%; EMC risk=6.

High: major change is expected in EMC performance exceeding 3dB in emissions or reducing immunity/ESD protection. Examples include changing an interface IC (e.g. RS232 to RS422); EMC risk=7, changing a crystal clock (e.g. 20MHz to 32MHz); EMC risk=8 or changing a microprocessor (e.g. 8051 to PIC) or main power supply switcher IC; EMC risk=9.

Risk Categories	Value
None	0
Low	1 - 3
Medium	4 - 6
High	7 - 9

Table 1: EDRA Risk Categories

The choice of risk level (R_x) is somewhat subjective, but most experienced designers and compliance engineers should be able to make an educated assessment of the likely effect of individual changes within a circuit on the EMC performance of a product on this 10-point scale. It is particularly true considering that the EDRA assessment is provided after testing and consequently information on the performance already achieved is available. Designers not familiar with the EMC risk of proposed changes can still use the technique as there are many examples available in a downloadable spreadsheet “knowledgebase” from many design projects that can be used as they stand (see below).

Impact Categories;

Impact categories are based solely on the application circuit to which the change is applied and the likelihood that these will be manifest outside of the system.

Low: impact is unlikely to be manifest outside of the product itself. Circuits affected are bias or steady state circuits and have no influence on the frequency content of the system or on the I/O; impact=1.

Medium: change will alter some frequency dependant content of the circuit or system, either filter circuit or oscillator circuit. Circuit does not directly interface with I/O but frequency change may be observed on supply line; impact=2.

High: circuits are directly connected to the I/O (including supply line), hence any change will be manifest to the external EM environment. Circuits may or may not affect frequency content; impact=3.

Impact Categories	Value
Low	1
Medium	2
High	3

Table 2: EDRA Impact Categories

The effect of the impact value (I_x) is to increase the effective risk value of those changes that are likely to directly affect measured EMC performance. Hence a change in de-coupling capacitor on an internal logic level will have a lower influence than a similar change on a serial data line IC connected to external circuits.

Retest Assessment

The sum of impact multiplied risk (equation 1) forms the quantitative retest assessment;

(1)

$$EDRA = \sum_{1}^{n} (R_x I_x)$$

The result should provide three retest categories; none, partial, full. The basic premise is that no re-testing would be required if the EDRA sums to less than 30, some re-testing should be performed if the EDRA is between 30 and 60 and full re-test if the EDRA result exceeds 60. The partial re-test could typically be a single test or a few specific tests that would be determined by the designer or EMC test engineer (e.g. ESD retest or radiated emissions).

Retest Status	Risk Assessment
No Retest	0<EDRA<30
Partial Retest	30<EDRA<60
Full Retest	60<EDRA

Table 3: Quantitative Retest Assessment

The risk assessment of changes must be cumulative between any testing to maintain the validity of the original results that the risks are being assessed against. This also prevents the false use of the EDRA technique by making a series of minor changes that individually do not suggest a retest but cumulatively exceed the suggested retest limit. After a full re-test the EDRA value is reset to zero for further design changes.

Design Examples

To illustrate the technique the following examples have been compiled.

Example A: Remote Sensor

A remote measurement sensor that has a discrete analogue stage, including a series diode protected input (reverse blocking) to a discrete transistor amplifier and reports data over a 2km RS485 interface. The sensor is to have a new input stage with a higher gain but reduced speed diode protection and the communications channel is to be cost reduced to a non-slew rate limited RS485 IC. The power supply filter is to have a smaller inductor and the decoupling capacitor for the micro-controller is reduced due to lower current consumption than expected.

Ref.	Design Change	Risk	Risk Value	Impact	EDRA
D1	Replace Schottky diode with small-signal version	MED	5	3	15
U7	Change from slew limited output version	HIGH	7	3	21
L6	Decrease inductance >50%	MED	4	3	12
Q7	Increase in gain by more than 25%	HIGH	7	2	14
C4	Decrease decoupling capacitor by <50%	MED	4	1	4
	FULL RETEST			Total =	66

Table 4: EDRA Example A

The EDRA produces a risk value of 66 (table 4) suggesting a complete retest. The interface IC may have a similar ESD protection built-in so that this test could be omitted from retest, but emissions will be effected by the change in slew rate. The most significant change is on the analogue input where the higher gain amplifier (transistor) represents a potential susceptibility increase and the diode protection will be slightly slower (hence worse) with the signal diode compared to the Schottky previously used. The changes in the input filter (inductor and the decoupling capacitor) are technically due to the lower than expected current requirement but will affect the conducted noise of the sensor as a whole.

The transistor stage proved to be the greatest problem and increased conducted noise by more than 6dB at 20MHz, the slew rate change of the IC had a 3dB increase close to 80MHz in the radiated result but was less significant than expected. The whole unit was still below the limits as there was a 16dB margin in the original emission results and over 20dB in the conducted measurements at the frequencies that were affected. A TCF was compiled with bench-top (pre-compliance) comparative conducted results and test laboratory radiated measurements only, ESD and immunity was not re-tested.

Example B: PC Plug-In Card

A video digitizing card with 10-bit analogue-to-digital converter (ADC), on-board real-time processing in an 80MHz DSP, DMA access to/from on-board video RAM shared with the host PCI bus. The card has only been resolving 6-bit video due to on-board noise and an analogue power plane is to be introduced to help resolve 8-bits at the ADC. The on-board decoupling capacitance is also to be doubled to assist with the ADC noise problem. The static pull-up resistors on the ADC that set some conversion conditions are accessible at the port for control over-ride, are to be reduced from 47kW to 10kW. The DSP has a new routine to pipeline the ADC data directly to memory before processing.

Ref.	Design Change	Risk	Risk Value	Impact	EDRA
C3	Increase decoupling capacitor by >50% <100%	MED	4	1	4
R6	Decrease value of pull-up to power rail by >50%	MED	4	3	12
PCB10	Introduce split to power plane	MED	5	3	15
A4	Add bus level data access routine	MED	5	2	10
	PARTIAL RETEST			Total =	41

Table 5: EDRA Example B

The EDRA produces a risk value of 41 (table 5) suggesting a partial retest. The interface components are likely to be of similar ESD tolerance even with reduced pull-up resistors and the power split, but these have a high impact factor as they are directly at the interface terminals (it is expected these will significantly improve EMC, justifying the high impact factor). The direct memory access routine increases bus level access frequency by a factor of 2 (hence increases transient load demand), but this is internal to the card (not on the I/O) and in the redesign is separated to the digital side of the power supply and helped by the increased decoupling capacitance.

The partial retest would probably be radiated immunity as this should indicate the magnitude of improvement on the ADC noise, but radiated emissions might also be retested to check the analogue/digital power split has been executed correctly in the PCB layout.

Example C: Laboratory Instrument

A small laboratory instrument has proved to have lower current consumption than originally predicted, hence the fuse used is to be lowered. The product is also being upgraded to store twice as many results in internal memory and a watchdog routine added to the microprocessor to assist with out-of-memory crashes experienced with some earlier units. The PCB is being revised to remove memory lines that were placed for a different memory device but that had never been utilized.

Ref.	Design Change	Risk	Risk Value	Impact	EDRA
X1	Reduce FUSE rating	LOW	1	3	3
U15	Replace memory with higher density device	MED	5	2	10
A1	Install software watchdog	LOW	1	1	1
PCB20	Remove non-used memory/data bus line	LOW	1	1	1
	NO RETEST			Total =	15

Table 6: EDRA Example C

The EDRA produces a risk value of 15 (table 6) suggesting no retesting is required due to these design changes. The main potential threat is the increased memory device that potentially increases the digital supply current, but overall the risk is still low as the addressing and data sizes are unchanged, hence dynamic supply requirements are unlikely to exhibit any significant change.

Examples Database

A knowledgebase of existing risk factors is available in an Excel spreadsheet for downloading from the internet (www.tridatacom.co.uk\EDRA.htm). The spreadsheet provides the basis of an expandable knowledgebase that can be contributed to by any reader and hence constructed from the experience of collective designs (without disclosing design

details). The risk and impact categories should be appropriate to most categories of electronic designs and the main differences between applications could be the total risk level at which retest is suggested.

It should be noted that some changes that improve the EMC performance will produce high EDRA values. This is consistent with the principle as the idea is to assess the impact on EMC regardless of it being beneficial or negative. This also prevents the idea that a change that degrades performance can be offset by one that improves it, typically the changes are unlikely to affect the same circuits of the same parametric results (e.g. test type or frequency). There are several anecdotal reports of perceived “good practice” causing poor results due to incorrect or inappropriate implementation. Conversely if a series of changes significantly improves the EMC performance, knowing this is of value and the changes can be implemented elsewhere if necessary and also the results provide greater EMC headroom for any future design changes.

Conclusion

The EMC design risk assessment (EDRA) technique proposed in this paper offers a simple low cost method of assessing the impact of design changes on the EMC performance of a circuit or product that has already been compliance tested. The method can be used to assess the effect of proposed changes or determine if the proposed changes are economically viable in light of their requirement for an EMC retest.

The EDRA method can only be applied to products that do not require certified approval (i.e. self-certified products only). The EDRA results can be used within a Technical Construction File (TCF) with existing test data to prove that design changes that have not been re-tested have at least been technically assessed by the design authority.

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